Full 3D Simulation of 6T-SRAM Cells for the 22nm Node

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Abstract—6T-SRAM cell designs for the 22nm node are compared via full 3-dimensional cell simulation with Sentaurus (v.2008.09), to allow the benefits of advanced MOSFET structures to be accurately assessed. Segmented MOSFET (SegFET) technology provides for enhanced read stability and write-ability, as compared to conventional planar and tri-gate technologies. It also provides for improved SRAM cell yield, primarily because of improved robustness to process-induced variations, and improved immunity to soft errors.

Keywords- MOSFET, 6-T SRAM, Variability, Single-event-upset.

I. INTRODUCTION

A challenge for continued SRAM cell area scaling is threshold voltage ($V_{TH}$) mismatch due to variability in transistor performance [1], which eventually degrades the minimum operating voltage of the SRAM array [2]. To suppress $V_{TH}$ variation due to random dopant fluctuations (RDF) and process-induced variations in device parameters, light channel surface doping via a retrograde or delta-shaped body doping profile [3] or a fully-depleted ultra-thin-body/multi-gate architecture [4, 5] should be used. To avoid the need for expensive SOI substrates or more complex fabrication processes [6, 7], the segmented bulk MOSFET (SegFET) design was proposed to reduce $V_{TH}$ variation [8-9]. In this work, the benefits of SegFET technology for 6T-SRAM are assessed via full 3-dimensional (3D) cell simulation, in contrast to conventional mixed-mode (device-circuit) simulation, with regard to read stability, write-ability, cell yield, and susceptibility to single-event-upset (SEU).

II. SEGMENTED BULK MOSFET STRUCTURE AND FABRICATION PROCESS

The SegFET structure and front-end-of-line fabrication process steps are illustrated in Fig. 1. The channel is divided into stripes of equal width ($W_{STRIPE}$), with very shallow trench isolation (VSTI) regions in-between the stripes. The VSTI depth should be deeper than the source/drain extension junction depth ($X_J$) in order to fully suppress source-to-drain leakage current underneath the VSTI, but can be much shallower than the STI used to isolate transistors so that the channel stripes do not have a large aspect ratio. Within each stripe, the doping profiles are identical to those in a conventional planar bulk MOSFET (Fig. 1a). A tri-gate structure is formed by recessing the VSTI by a small amount ($H_{STRIPE}$) prior to gate stack formation; together with a retrograde channel doping profile (peaked at a depth $T_{Si}$), it provides for superior electrostatic integrity. The SegFET fabrication process (Fig. 1b) is identical to a conventional bulk MOSFET fabrication process, except that a corrugated substrate is used as the starting material. Since the features on the corrugated substrate are geometrically very regular, small-pitch and high-resolution patterning techniques such as multiple patterning or spacer lithography [11] can be readily used to achieve stripes of uniform width with very fine pitch. For improved layout area efficiency, the stripe spacing ($W_{SPACING}$) can be less than $W_{STRIPE}$.

III. 6-T SRAM CELL DESIGNS

Fig. 2 shows the scaling trend for 6T-SRAM cell area. Based on recent publications [12-16], the dimensions for
22nm-node cells (Table 1) were selected for this study. The pull-up (α) ratio and cell (β) ratio of the SegFET SRAM cell design, with 2W\text{stripe} = 40nm, H\text{stripe} = 10nm, and W\text{spacing} = 15nm for the pull-down devices, are comparable to those of the other SRAM cell designs. The gate sidewall spacer width (~10nm), with an upper limit imposed by the gate-to-contact pitch, and the source/drain extension junction depth (~10nm) are each optimized to achieve good static noise margin (SNM) [17] and write-ability current (Iw) [18].

To achieve the same V\text{TH,lin} as for the planar devices, the gate work-function is set to 4.3eV for the SegFETs. The SNM and Iw values for each cell design were obtained from simulations (Fig. 4) using advanced physical models including the density-gradient transport model and drift-diffusion model. As shown in Fig. 5, the SegFET cell has the highest SNM across the entire range of V\text{DD} values, and it is sufficient (≥0.2×V\text{DD}). The SNM at V\text{DD} = 1.1V is smaller for the tri-gate cell as compared to the planar cell due to a weaker body effect in the pass-gate devices [10].

Due to its superior electrostatic integrity, the SegFET is more robust to global and local variations. Figs. 6a and 6b show the 6T cell layout and 6T SRAM circuit schematic are shown to indicate the parameters designated in the table.

### IV. GLOBAL/LOCAL VARIATION ANALYSIS

A sensitivity analysis was performed to assess the benefit of SegFET technology for improving SRAM cell yield using the concept of cell sigma, defined as the minimum amount of variation for read/write failure [10]. As shown in Fig. 6c, the SNM cell sigma for the SegFET cell is ~8, which is a 3-sigma improvement over the planar cell. The minimum V\text{DD} that meets the six-sigma yield requirement for both SNM and Iw is V\text{DD} = 0.9V.

### V. SIMULATION OF SINGLE-EVENT-UPSET

SRAM cell soft-error tolerance was evaluated using an inverter model in [19]. The high (‘1’) storage node is the region of the cell that is most sensitive to a particle strike, because the drain junction of the corresponding pull-down device is reverse-biased so that the probability of collecting generated electron-hole-pairs (EHPs) in the drain depletion region is relatively high. In this work, soft-error tolerance is studied via transient simulation of complete 3D 6T-SRAM structures. First, the cell is written and then the data is held. Then, a heavy ion beam (Fig. 7) is made to vertically impinge on the high (‘1’) storage node at time t = t\text{impact}, for each of the different SRAM cell designs. Due to the funneling effect [20], a parasitic thyristor turns on to short the drain node to the source node. This is evident in Figs. 8a and 8b, which show compare short-channel effects and narrow-width effects, respectively, for the SegFET vs. planar MOSFET structures. Variation due to RDF was evaluated via atomistic simulations [9]: σ(V\text{TH}) ~ 25mV and 28mV for n-channel and p-channel SegFET/tri-gate devices, respectively; σ(V\text{TH}) ~ 45mV and 49mV for the n-channel and p-channel planar devices, respectively.
Fig. 4. 3D 6-T SRAM cells simulation results: (a) butterfly plots and (b) write-N-curves for Planar, Tri-gate, and SegFET technologies. Each butterfly curve took ~6 hrs to simulate using an AMD64 machine (8 cores).

Fig. 5. (a) SNM and (b) $I_w$ vs. $V_{DD}$. The SegFET cell has higher SNM across the range of $V_{DD}$. The tri-gate cell has better SNM at lower $V_{DD}$ (<0.9V), as compared to the planar cell.

Fig. 6. SegFET vs. planar MOSFET comparison: (a) $V_{TH,lin}$ vs. $L_g$ (b) $V_{TH,lin}$ vs. $W$ (c) SNM cell sigma (d) $I_w$ cell sigma.
Segmented MOSFET (SegFET) technology is projected to achieve enhanced read stability and write-ability, improved SRAM cell yield, and improved immunity to soft errors.

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**REFERENCES**


**VI. CONCLUSION**

Full 3D 6T-SRAM cell simulations are used to assess the benefits of advanced MOSFET structures at the 22nm node.