A Low Voltage Steep Turn-Off Tunnel Transistor Design

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***Abstract*—A new tunneling transistor structure is introduced that offers several advantages over prior designs. Notably, tunneling area is substantially increased. Turn on/off swing is improved by engineering doping profile to ensure tunneling initiates in high electric field region. TCAD simulations explore the critical design considerations. The concept of heterojunction tunneling is introduced as a means to achieve low effective band gap and low voltage operation for the design in consideration.**

I. Introduction

Increasing power consumption presents a major problem for future ICs. A transistor that can operate below 0.5 V supply is highly desirable. Maintaining large I_{on}/I_{off} ratio at such low V_{dd} is a challenge for MOSFET given the 60 mV/decade subthreshold swing limit. This limit governs the turn off/on of any device based on flow of carriers over an energy barrier.

Band-to-band tunneling (BTBT) is one process not subject to this limitation. Researchers have long explored the BTBT transistor [1-2]. However, all have relied on the same basic structure -- the gated PN diode. This conventional structure for an n-type FET is shown in Fig. 1. The location of tunneling is indicated by the arrow at the edge of the source region. The transistor "turns on" when the gate voltage exceeds the overlap voltage, V_{ov}, defined as the voltage at which there are alignment of states between valance and conduction band, permitting electrons to tunnel and drift across the channel to the drain.

Unfortunately, prior experiments for this structure have shown disappointingly low drive current and poor subthreshold swing. We propose a new transistor design that provides significant improvement in on-current and swing.

II. Proposed Tunnel Transistor Structure

Fig. 2 shows the new proposed transistor design. [3] The P+ source overlaps a fraction of the gate and includes an ultra shallow N+ pocket. Two tunneling paths exist in this structure. $V_{ov,1}$ is the overlap voltage for tunneling between the P+ source and N+ pocket. $V_{ov,2}$ is for tunneling between source edge to channel as in the prior structure. This design requires that $V_{ov,1} < V_{ov,2}$, i.e. the source to pocket P+/N+ tunneling path dominates. This approach has two large advantages compared to prior work. (1) The tunneling area is determined by the pocket length L_{pocket}, in contrast to the inversion layer thickness in the conventional design. This allows for significantly larger on-current. (2) Electric field is already very high at P+/N+ pocket region when the overlap condition $V_{ov,1}$ is satisfied. This results in very rapid rise of

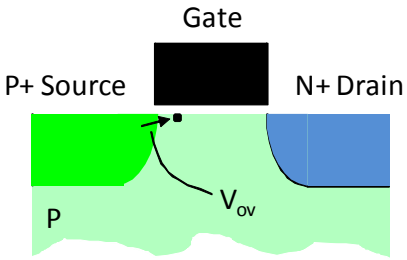

Fig. 1: Structure of conventional n-type tunnel transistor. The overlap voltage, $V_{ov,}$ is the gate voltage at which tunneling occurs when states are aligned.

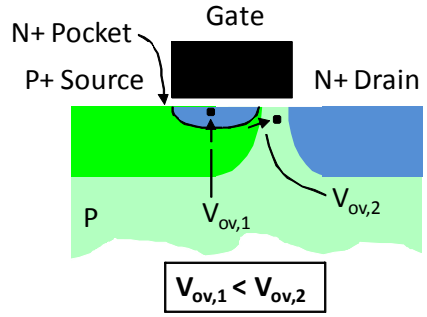

Fig. 2: Proposed n-type tunnel transistor with ultra shallow pocket. $V_{ov,1}$ is the overlap voltage for source/pocket tunneling. $V_{ov,1}$ must be less than $V_{ov,2}$ for steep "turn on".

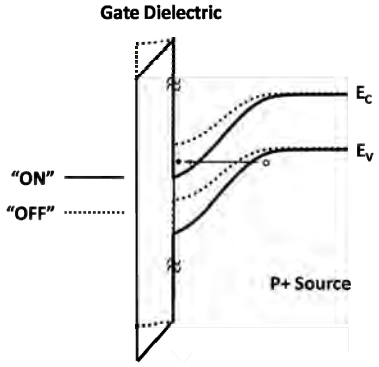

Fig. 3: Band diagram of proposed tunnel transistor in "on" and "off" states. No alignment of states in "off" condition.

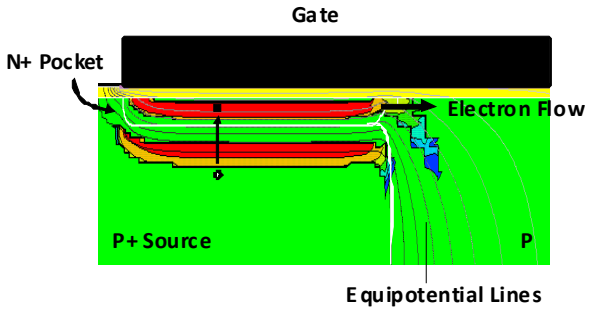

Fig. 4: BTBT generation rate contours for proposed tunnel transistor in "on" state. Lower and upper rate contours represent hole and electron generation.

the tunneling current and consequently very steep subthreshold swing over many decades of current.

The simulated energy band diagram is shown in Fig. 3 in the "off" and "on" state, i.e. V_g = 0, V_{dd}. During the "off" state there is no overlap, hence zero tunneling current. When the device is turned "on" the gate raises the potential in the N+ pocket through capacitive coupling, causing valance electrons to tunnel from the P+ source to the pocket. The generated electrons drift to the drain to be collected as drain

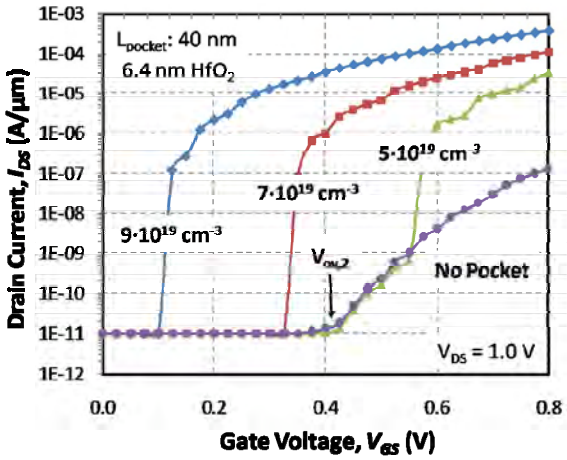

Fig. 5: Importance of pocket doping to achieve $V_{ov,1} < V_{ov,2}$ criteria. Pocket dose lowers overlap voltage $V_{ov,1}$.

current. Fig. 4 is the simulation output showing uniform BTBT generation rate across the length of the pocket. The upper contours represent electron generation, while the lower is for holes.

III. Proposed Tunnel Transistor Design

MEDICI simulator is used with default silicon BTBT model, which has shown reasonable agreement with prior tunneling data. [3] In order to satisfy the $V_{ov,1} < V_{ov,2}$ design criteria, the pocket dose must be sufficiently high. In Fig. 5 the N+ pocket doping concentration is varied for fixed 3 nm junction depth. The pocket dose shifts $V_{ov,1}$ to lower voltages. The simulated swing is < 10 mV/decade. Also shown is simulation for the identical structure without the pocket to identify $V_{ov,2}$ as labeled on the plot. In this case, when pocket doping concentration is $5x10^{19}$ cm^{-3} and lower, $V_{ov,1} > V_{ov,2}$ and the turn on characteristics are degraded.

Equally important is the junction depth of the N+ pocket. Fig. 6 shows relative degradation in on-current when junction depth is increased for fixed pocket dose. This is

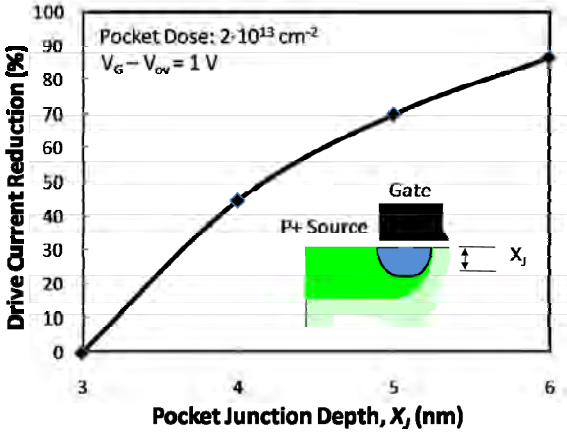

Fig. 6: Increased pocket junction depth for fixed dose reduces I_{on} due to reduced gate capacitive coupling.

because peak electric field decreases when the junction depth is increased. Fig. 7 shows the importance of the lateral positioning of the N+ pocket. Defined as the offset, a positive value corresponds to the pocket extending beyond the source edge. This results in degraded swing because now $V_{ov,1} > V_{ov,2}$, since the pocket dose equally shifts both quantities by the same amount. Proper design should ensure the N+ lateral pocket edge terminates before the source edge profile.

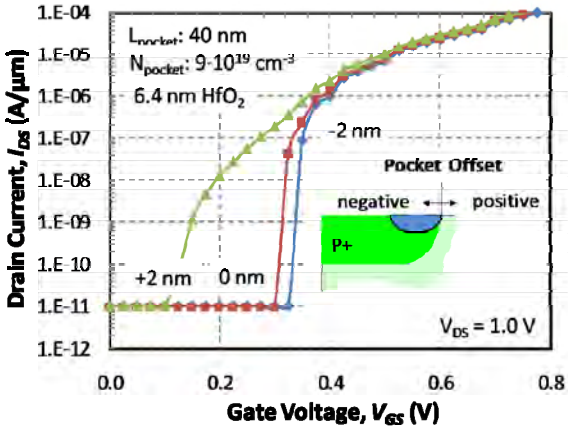

Fig. 7: Impact of pocket offset with respect to edge of the source on "turn on" characteristics. Negative offset is defined as the pocket enclosed by the source doping.

Fig. 8 shows that reducing the band gap E_g of the tunnel junction material provides a needed path for V_{dd} scaling. Unfortunately, even Ge band gap only allows scaling to 0.5 V with large I_{on}. Further V_{dd} scaling requires ultra-low-E_g

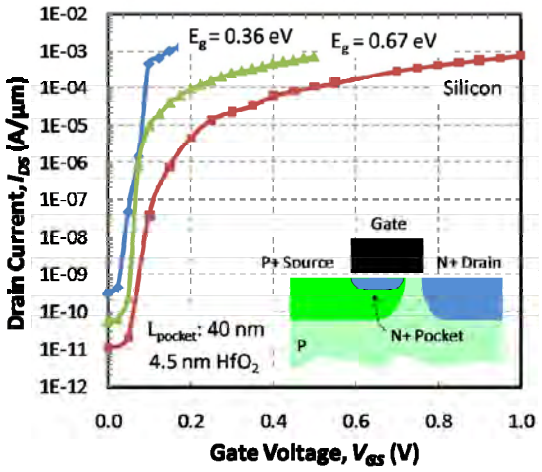

Fig. 8: Reducing E_g of the tunnel junction allows for supply voltage reduction with large drive current.

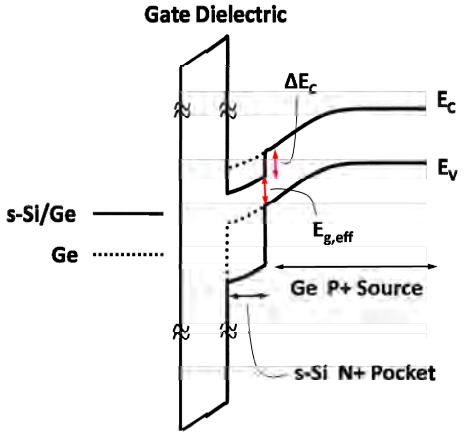

Fig. 9: Large E_c offset, determined by the amount of strain in Si cap, allows for low effective tunnel band gap.

low-effective-mass materials which have technology compatibility and low density-of-states issues.

IV. Hetero-Tunnel Transistor Concept

Fig. 9 shows a new way to reduce V_{dd} without ultra-low-E_g low effective-mass materials in the proposed design. [4] Tunneling still occurs between N+ pocket / P+ source but now a different material is introduced for the pocket. Carries

Ref.	ΔE_c	ΔE_v	$E_{g,s\text{-}Si}$	$E_{g,eff}$
[6]	0.55	0.31	0.42	0.19
[7]	0.57	0.25	0.35	0.17
[8]	0.58	0.21	0.37	0.16

Table I: E_c and E_v offset, strained silicon band gap and effective band gap (eV) of pseudomorphic Si on Ge.

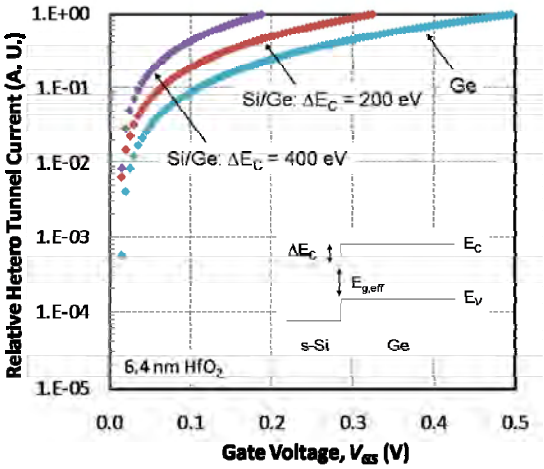

Fig. 10: Relative Si/Ge hetero-tunneling current I_d-V_g generated from 1D hetero WKB model for various E_c offsets compared to pure Ge tunnel current. Larger offset or smaller effective band gap allows for smaller gate voltage.

tunnel across this hetero-junction with a lower effective band gap, $E_{g,eff}$. Strained silicon atop relaxed germanium is an interesting system to explore. Table I summarizes the reported band offset and effective band gap of strained Si grown on germanium substrate. The E_c offset can be as large as 0.5 eV when the Si is fully strained, resulting in effective E_g as low as 0.2 eV. Such reduction in the band gap allows a large increase in the tunneling current as can be seen in Fig. 10. Moreover, the same drive current can be attained in much smaller supply voltage. The detailed physics of hetero-tunneling is not implemented in commercial TCAD simulators. The one-dimensional hetero-tunneling current was calculated using the WKB approximation and Franz two-band model for imaginary wavevector in MATLAB. [5] All possible tunneling paths were taken into account at each bias point. This includes paths which are entirely in silicon, germanium or through both materials as is the case for the $E_{g,eff}$ path. A more thorough explanation of this model will be presented in future publication. Table II shows the orientation dependence of the strain showing that growth on (100) substrate gives the smallest effective band gap.

V. Summary

A new tunnel transistor structure is proposed that improves both the subthreshold swing and drive current. Simulations demonstrate subthreshold swing can be less than 10 mV/decade. Germanium provides scalability down to 0.5 V with large I_{on}. Utilizing heterojunction tunneling with low "effective" band gap may provide scalability below 0.5 V.

	(100)	(110)	(111)
$E_{g,s\text{-}Si}$	0.55	0.31	0.42
$E_{g,eff}$	0.57	0.25	0.35

Table II: Orientation dependence of the effective band gap (eV) of strained Si on Ge [9].

ACKNOWLEDGMENT

This work is supported by DARPA under the STEEP program.

REFERENCES

[1] W. M. Reddick et al., Applied Physics. Letters, vol. 67(4), pp. 494–497, 1995.

[2] C. Aydin et al., Applied Physics. Letters, vol. 84(10), pp. 1780-82, 2004.

[3] C. Hu et al., *Invited* VLSI-TSA, Taipei, Taiwan, April, 2008.

[4] A. Bowonder et al., International Workshop on Junction Technology, pp. 93-96, 2008.

[5] W. Franz, Handuch der Physik, Springer-Verlag, Berlin, 1956.

[6] C. G. Van der Walle et al, Physics Review B, vol. 38(8), pp.5621-5634, 1986.

[7] M. M. Rieger et al., Phyics. Review B, vol. 48(19), pp.14276-14287, 1993.

[8] L. Yang et al., Semiconductor Science Technology. vol. 19(10), pp.1174-1182, 2004.

[9] Band Structure Lab, available at www.nanohub.org