Lateral Ge/SiGe/Si hetero-channel p-type MOSFETs

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***Abstract* —To further device scaling, a new hetero-channel MOS device is considered. A novel Ge/SiGe/Si lateral hetero-channel p-FET that can significantly reduce band-to-band tunnelling (BTBT) leakage, retain high current drivability, and good electrostatics is introduced in this paper. Through detailed BTBT model in PDE simulators the on-current and off current in p-FETs are analyzed. The simulation results show one-order of magnitude reduction (>20) in minimum off current and high drive current. Lateral hetero-channel p-FET provides a promising solution for future highly scaled CMOS technology.**

Index Terms* — *SiGe; field effect transistor; BTBT leakage; device scaling

I. INTRODUCTION

The scaling of MOSFETs has played an important role in improving digital integrated circuit performance and to continue this historical trend, higher mobility channel material is required to achieve sufficient virtual source velocity [1]. Ge-based p-FETs have superior hole mobility so are considered to be performance-enhanced replacements for the pure Si channel devices for digital and analog applications [2, 3]. However compared with Si, Ge also has a smaller bandgap and higher dielectric constant leading to significant BTBT leakage and a severe short channel effect (SCE), which fundamentally limits the scability. Si-strained SiGe/Si p-type double gate FETs were proposed and can be a promising solution to reduce BTBT leakages in Ge-FETs [2]. However in this structure the double gate Si/Ge/Si structure is required to get enough quantum confinement, which is challenge for current fabrication technology. This paper introduces a novel hetero-channel MOS that does not rely on quantum confinement effect and can dramatically reduce BTBT leakage, perfect electrostatic control, and achieve high drive current. This paper contains three sections in which the device structure of lateral hetero-channel FET and the working principles are discussed. Then off-current characteristics are addressed, especially BTBT leakage. Finally, on-current characteristics are noted. Through the study of this paper, the performance of the hetero-channel FETs can be a promising solution for high-performance digital applications.

II. DEVICE STRUCTURE AND WORKING PRINCIPLES

A channel in the source and drain side require different material characteristics. On-current characteristics depends more at the source side characteristic of a channel such as virtual source velocity and low-field mobility. On the other hand BTBT leakage is mainly depends on the drain side characteristics such as the band gap and drain-side electrical field. A hetero-channel MOS device can be a promising solution that can significantly reduce BTBT leakage and provide a high drive current. The schematic of the lateral hetero-channel FET, introduced in this paper, is shown in Fig. 1 (a). In this paper we focus particularly on SiGe lateral hetero-channel p-FET which consist a hetero-channel: high mobility narrow band gap material, Ge at the source and large band gap material, Si at the drain side. The Ge mole fraction gradually decreases from the end of the channel to drain as shown in Fig. 1(b). The goal is to use high mobility near the source and larger bandgap near the drain. This combines the advantage of the high low field mobility of Ge with the larger band gap of Si.

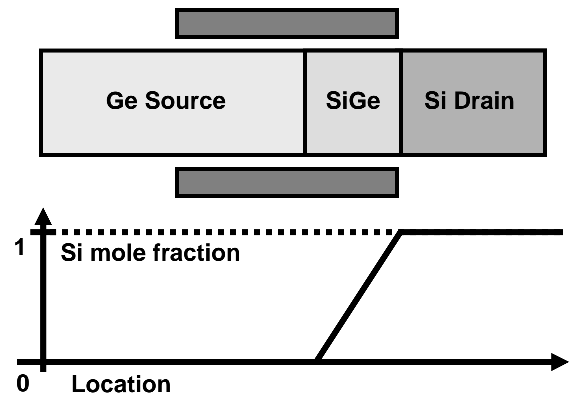

Fig. 1. (a) Schematic plot of a lateral Ge/SiGe/Si heterochannel MOS device and (b) Si mole fraction along channel direction.

The band diagrams of the lateral hetero-channel p-FET are shown in Fig. 2. As can be seen from the figure, in the off state the larger bandgap near drain can reduce BTBT leakage. Moreover smaller permittivity of Si can decrease electrical field near drain to improve SCE. On the other hand in the on state the effect of graded SiGe/Si valence band offset becomes negligible and the carrier transport is smooth.

III. OFF-STATE CHARACTERISTICS

In off state the high electrical field from the drain to gate causes large band bending and leads to BTBT leakage. Compared with Si high mobility materials such as Ge, InSb, and InAs usually have smaller bandgap and higher permittivity so BTBT leakage becomes much more significant

in this kind of devices. Moreover the higher permittivity of high mobility materials can cause worse SCE and degrade subthreshold slope.

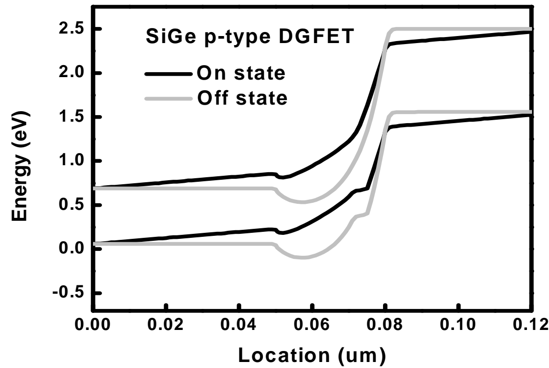

Fig. 2. Band diagrams of a hetero-channel FET along horizontal direction.

Through BTBT model in Medici off-current characteristics of various hetero-channel FETs can be analyzed. Table I gives a summary of simulated device structure parameters. As shown in Fig. 3 compared with Ge p-FET the lateral heterochannel SiGe p-FETs can effectively suppress the BTBT leakage by one order of magnitude (>20). The reasons for such significant BTBT leakage reduction are mainly due to the larger bandgap and smaller drain-side electrical field. To verify the effect of drain side material for BTBT leakage, Fig. 3 shows off-current characteristics for different drain-side Si mole fractions. As can be seen, the minimum off-current strongly depends on drain-side Si mole fraction.

Devices	EOT	Gate length	Channel doping
SiGe p-FET	1nm	30nm	1e15 cm^{-3}

Table I. summary of simulated device parameters.

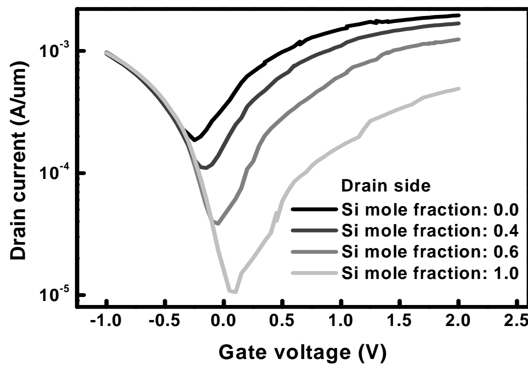

Fig. 3. Simulated I_d-V_g characteristics for different drain side Si mole fractions.

IV. OFF-STATE CHARACTERISTICS

The main concern with lateral hetero-channel FETs is the reduced drive current due to smaller mobility near the drain side and the SiGe/Si bandgap offset in the carrier transport path. Through PDE solvers on-current characteristics can be studied. From Fig. 3 it can be seen that on-current is not sensitive to drain-side Si mole fraction. To accurately benchmark the on-current characteristic, for a given gate length, L_g and oxide thickness on-current simulations are performed by varying transition regions, L_t. From the small plot in Fig. 4 the simulation space can be understood. Fig. 4 shows on-current versus L_t. As seen from Fig. 4, on-current exhibits a "sweet spot" around the L_t of 5.5 nm, which is the result of two effects: (1) for a large L_t the low mobility region increases and can decrease Ion and (2) for the small L_t the effect of SiGe/Si band offset in the transport path becomes more significant. The optimization of L_t for on-current exists in hetero-channel FETs.

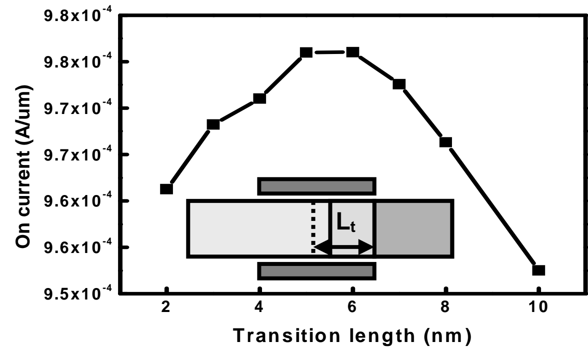

Fig. 4. Simulated on-current for different transition regions.

V. CONCLUSIONS

A novel SiGe lateral hetero-channel p-FET that can significantly reduce BTBT leakage, retain high current drivability and keep good electrostatic control is introduced. In particular SiGe lateral hetero-channel p-FETs with 30nm gate length have been thoroughly analyzed. The results show one order of magnitude reduction in minimum off-current, high drive current, and excellent electrostatic control. The lateral hetero-channel p-FET is a promising solution for future highly scaled devices.

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