A Surface Potential Based Poly-Si TFT Model for Circuit Simulation

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***Abstract*— We have developed a compact model of poly-Si TFTs based on complete surface-potential descriptions, including carrier trapping. The model was shown to be reliable for predicting high-speed circuit performances.**

Keywords- Compact Model; Thin Film Transistor; Trap Modeling

I. INTRODUCTION

Poly-silicon (poly-Si) thin film transistor (TFT) circuits, which are monolithically integrated on system-on-glass (SOG) displays, have received a great deal of attention as attractive devices for use in versatile ubiquitous appliances. In addition, recent progress in crystallization technology and device scaling are enabling the fabrication of high performance TFTs for high-speed /high-frequency circuits on display substrates. [1][2]

An accurate compact model of the poly-Si TFT is prerequisite for using these advanced technologies in real applications. To capture features of the poly-Si TFT, we developed a compact model based on the complete surface-potential-based description that solves the potential distribution down to the insulating substrate. Our model reproduced the high performance of the TFT circuit measurements with high accuracy.

II. DEVICE STRUCTURE AND TFTS SPECIFIC FEATURES

Figure 1 shows a typical TFT structure. In comparison with conventional MOSFETs, TFTs have following specific features, which must be considered in compact modeling.

1) A considerable number of traps occurs at the grain boundaries of the poly-Si layer. The trapped carriers affect *I-V* characteristics of TFTs significantly, as shown in Figure 2.

2) Because of the insulating substrate, the potential of the backside of the poly-Si layer is floated and varies with the voltages applied.

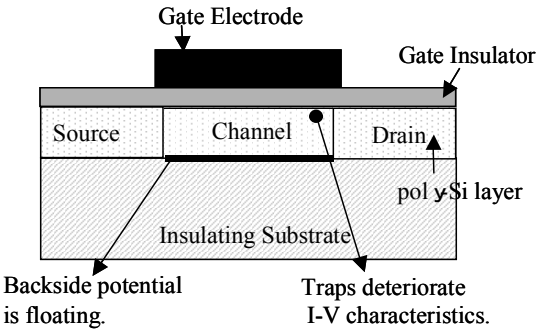

Figure 1. Typical structure of poly-Si TFT

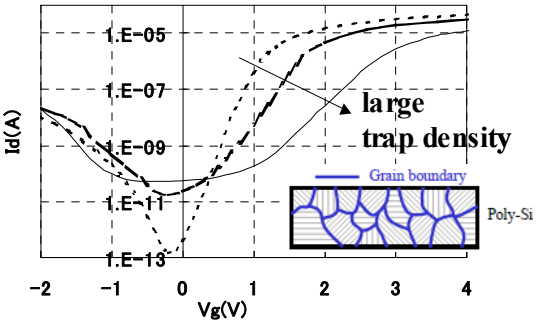

Figure 2. Effect of traps on I-V characteristics
By 2D device simulation.
Inset shows grain boundaries in Poly-Si.

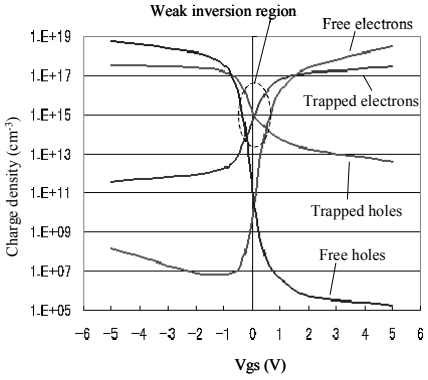

Figure 3. Density of charges at channel center surface versus gate voltage. Result of 2D device simulation for an n-channel TFT.

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III. MODELING APPROACH

A. Poisson Equation

Based on the 2D device simulation results (Figure 3), we decided that both trapped electrons and holes should be taken into account. Therefore, to describe the TFT features, we solved the Poisson equation as (1) :

$$\nabla^2\phi = -\frac{q}{\varepsilon_{Si}}\left(p - n + N_D^+ - N_A^- + N_{TD}^+ - N_{TA}^-\right) \quad (1)$$

where ϕ, ε_{Si}, and q are the potential, the silicon permittivity, and the electron charge, respectively. N_D^+, N_A^-, p, and n are concentrations of the donors, the acceptors, the holes, and the electrons, respectively. N_{TD}^+ and N_{TA}^- are the ionized donor-type and the ionized acceptor-type trap density, respectively.

B. Trap Modeling

1) Ionized trap density at the poly-Si surface

In order to handle both acceptor-type and donor-type traps using a simplified model, we approximated the density of acceptor-type trap states $g_A(E)$ and donor-type trap states $g_D(E)$ as (2) and (3), respectively (see Fig. 4) [3]:

$$g_A(E) = g_C \exp\left(\frac{E - E_C}{E_S}\right) \quad (2)$$

$$g_D(E) = g_C \exp\left(\frac{E_V - E}{E_S}\right) \quad (3)$$

where E_C and E_V are the energy of the bottom of the conduction band and the energy of the top of the valence band, respectively. E_S and gc are the inverse slope of the trap states and the trap states density at E_C and E_V, respectively.

Integrating the product of the Fermi-Dirac distribution function and each of (2) and (3) across the band gap, equations to describe the density of ionized acceptor-type traps and donor -type traps are obtained as (4)-(6) [4]:

$$N_{TA}^- = N_{tK} \cdot \exp\left(\frac{E_{Fn} - E_C}{E_S}\right) \quad (4)$$

$$N_{TD}^+ = N_{tK} \cdot \exp\left(\frac{E_V - E_{Fp}}{E_S}\right) \quad (5)$$

$$N_{tK} = gc \cdot E_S \cdot \frac{\frac{k \cdot T}{q \cdot E_S}}{\sin\left(\frac{k \cdot T}{q \cdot E_S}\right)} \quad (6)$$

where E_{Fn} and E_{Fp} are the quasi-Fermi energy for electrons and holes, respectively. T and k are the lattice temperature in kelvin and the Boltzmann constant, respectively.

For compact modeling, the relation is rewritten with the quasi-Fermi potential, which is considered to be a function of electrostatic potential. With 2D device simulations, we found that the relationship at the surface of the poly-Si layer can be described as (7) and (8):

$$\left[E_{Fn} - E_C\right]_{x=0} = \tan^{-1}\left(\frac{V_g - V_{FB} - \phi_S}{TOX \cdot E_{s-K}}\right)\frac{Efn_{MAX} - Efn_{MIN}}{\pi} - Efn_0 \quad (7)$$

$$\left[E_V - E_{Fp}\right]_{x=0} = \tan^{-1}\left(-\frac{V_g - V_{FB} - \phi_S}{TOX \cdot E_{s-K}}\right)\frac{Efn_{MAX} - Efn_{MIN}}{\pi} - Efn_0 \quad (8)$$

where x is the position from the surface in direction perpendicular to the poly-Si layer. TOX, V_{FB} , and ϕ_s are the gate insulator thickness, the flat band voltage, and the surface potential, respectively. $E_{S\text{-}K}$, Efn_{MAX}, Efn_{MIN} , and Efn_0 are fitting parameters.

Figure 5 shows a comparison of 2D device simulation results and those of our model. From (4)-(8), the ionized trap density at the poly-Si layer surface, N_{t0}, is obtained as a function of the surface potential as (9).

$$N_{t0} = \left[N_{TA}^- - N_{TD}^-\right]_{x=0} \quad (9)$$

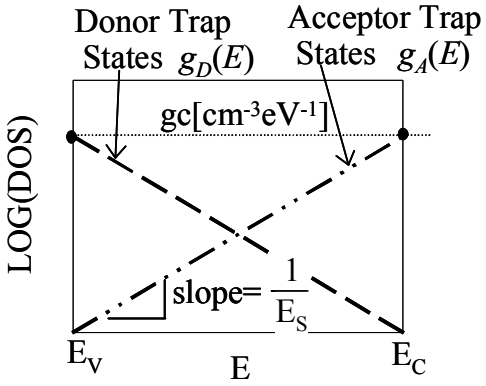

Figure 4. Simplified model of distribution of trap states across the band gap.

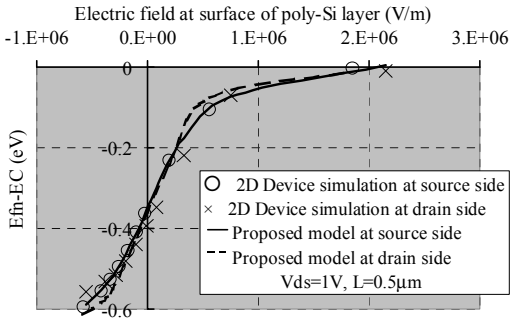

Figure 5. Calculated Efn-EC as a function of the electric field at the poly-Si layer surface, by 2D device simulations and by the proposed model.

2) Ionized trap density profile in the poly-Si layer

In order to solve the Poisson equation with the trapped charge, we need to know the ionized trap profiles in the poly-Si layer. Figures 6 and 7 show the calculated results of ionized trap density as functions of potential and of x. Based on the results, we adopted an approximate description for the ionized trap density N_t as (10) and (11):

$$N_{TA}^{-} - N_{TD}^{+} = N_t(\phi) = N_{t0} \cdot \frac{\phi - \phi_b}{\phi_S - \phi_b} \tag{10}$$

$$= N_t(x) = N_{t0} \cdot \exp\left(-\frac{K}{t_{Si}} x\right) \tag{11}$$

where ϕ_b is the backside potential of the poly-Si layer. K is a fitting parameter and t_{Si} is the thickness of the poly-Si layer.

C. Backside Potential

Next, integrating depletion charges and trap charges in the poly-Si layer from the surface to the backside, the relation between the surface potential and the backside potential are derived as (12) and (13):

$$\phi_b = \phi_S - \phi_{sb0}\left(1 - \exp\left(\frac{-\phi_S}{\phi_{sb0}}\right)\right) \tag{12}$$

$$\phi_{sb0} = \frac{q}{\varepsilon_{Si}} t_{Si}^2 \left\{ \frac{N_A}{2} + \frac{\exp(-K)(K-1)-1}{K^2} \cdot N_{t0} \right\} \tag{13}$$

where N_A is the impurity concentration in the poly-Si layer.

D. Surface Potential Calculation

The trap model (10) is added into (1). Then, the surface potential is calculated by solving (1) with the Gauss law as (14):

$$C_{OX}(V_g - V_{FB} - \phi_S) = \sqrt{\frac{2q\varepsilon_{Si}N_A}{\beta}}\left[\exp(\beta\phi_S) - \exp(\beta\phi_b) + \beta(\phi_S - \phi_b) + \frac{ni^2}{N_A^2}\{\exp(\beta\phi_S) - \exp(\beta\phi_b)\} + \frac{\beta N_{t0}}{N_A}\frac{(\phi_S - \phi_b)}{2}\right]^{\frac{1}{2}} \tag{14}$$

where C_{OX}, V_{FB} , β, and ni are the gate insulator capacitance per unit area, the flat band voltage, the inverse thermal voltage, and the intrinsic carrier concentration, respectively.

Substituting ϕ_b by (12), (14) is solved iteratively after HiSIM (Hiroshima University STARC IGFET MODEL) approach [5]. Drain current, charges and other device characteristics are calculated using these potential values.

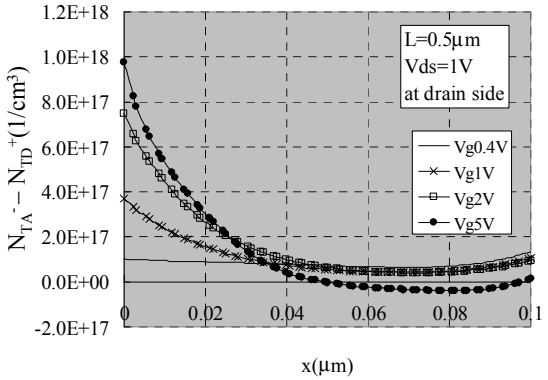

Figure 6. Calculated ionized trap density in the poly-Si layer as a functin of position x.(by 2D device simulation)

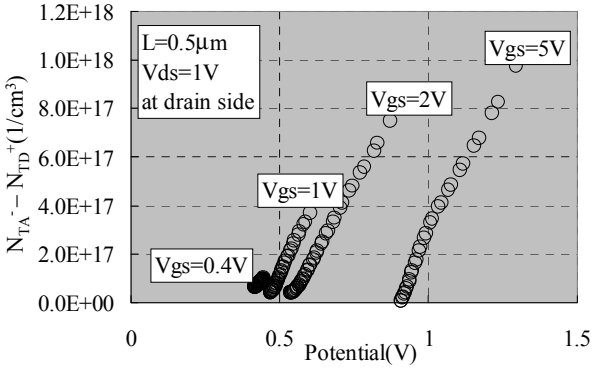

Figure 7. Calculated trap charge density in the poly-Si layer as a function of potential.(by 2D device simulation)

IV. SIMULATION RESULTS

A. I-V characteristics

We compared calculated *I-V* characteristics from the developed model to measurements. Figure 8 shows the comparison for gate length (L) of 2 and 0.5 μm as a function of gate voltage, V_{gs}, and drain voltage, V_{ds}. As shown in Figure 9, effects of trap charges on I-V characteristics are well modeled.

B. Circuit Simulation Results

Figure 10 shows a comparison of measured and calculated oscillating frequency of a 7-stage ring oscillator. Figure 11 shows a comparison of measured and calculated voltage gains of a high-speed amplifier for a LVDS receiver[6][7]. These circuits' performances are extremely high in comparison to conventional poly-Si TFT circuits, because they consist of high performance of TFTs with reduced channel length (0.5-1.0μm) and high mobility poly-Si layer crystallized by PMELA(Phase Modulated Eximer Laser Annealing) method [1]. It is notable that simulation results are accurate not only for *I-V* characteristics but also for high-speed circuit simulations.

V. CONCLUSION

By introducing a new trap model and solving the potential distribution along the substrate depth direction, we have

developed a compact model for poly-Si TFTs. We have confirmed accurate simulation of I-V characteristics and accurate prediction of high-speed circuits. Therefore this compact model will be of value for designing next-generation SOG technologies.

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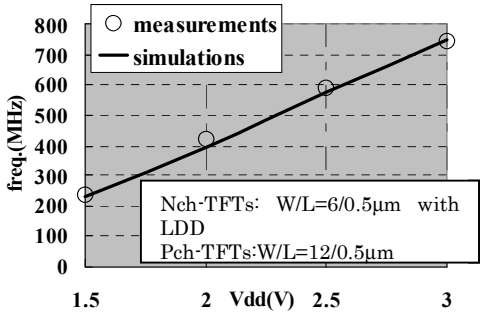

Figure 10. Frequency-Vdd characteristics in a 7-stage ring oscillator.

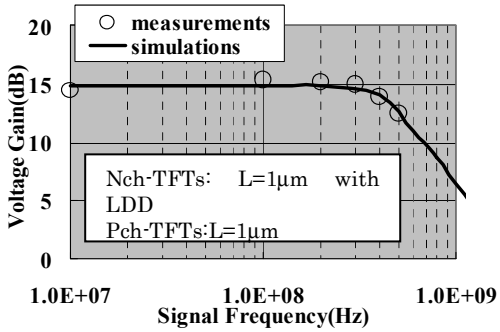

Figure 11. Voltage gain-Signal frequency in a high speed amplifier for LVDS receivers.

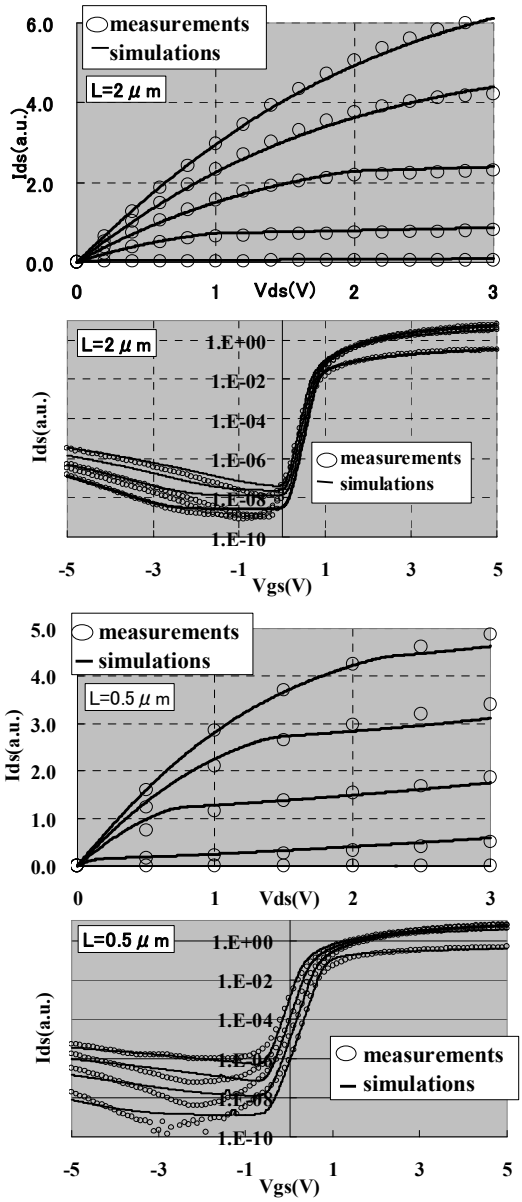

Figure 8. Comparison of measured (circles) and simulated (lines) drain current characteristics as a function of drain voltage and gate voltage.

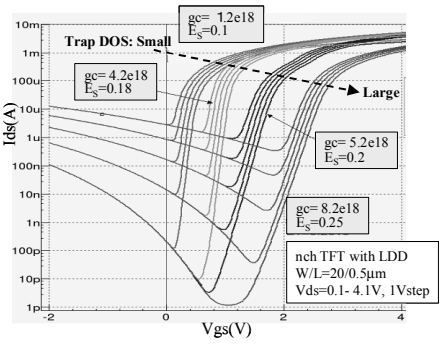

Figure 9. Comparison of measured (circles) and simulated (lines) drain current characteristics as a function of drain voltage and gate voltage.