Synthetic Soft Error Rate Simulation Considering Neutron-induced Single Event Transient from Transistor to LSI-chip level

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***Abstract*— Soft error phenomena induced by the Sea-level cosmic neutron have been investigated by using a simulation system that covers from an individual MOSFET device level to an LSI-chip level. This system consists of the several kinds of simulation codes/tools, such as a mixed-mode 3D device simulator, SPICE circuit simulator, and analyzing tools of gate-level net-lists. A comprehensive practical simulation flow is demonstrated in this paper on commercial 90nm generation logic devices and standard-cells.**

Keywords; Soft Error; simulation; Single Event Transient

I. INTRODUCTION

Recently, soft error phenomena induced by cosmic neutron are getting much attention not only on large-scale random-access memory application but also combinational-logic circuits. The latter error phenomena in the logic circuits are considered as the erroneous signal propagation which is called a Single-Event-Transient (SET) effect and is becoming an interesting topic of the future scaling issues [1].

Understanding the cause of the SET and quantitative analysis/design-improvement are not always easy tasks if we could merely see accelerated neutron-beam irradiation test or any long-term field test, since these tests only could tell us system-level failure rates which are not easy to be decomposed into several fundamental design-level of transistor, primitive circuit cells, and functional synthesis on certain processor architecture design for instance.

Therefore, we have developed our comprehensive simulation system for the soft error analysis considering the SET effect by using several different kinds of CAD tools.

II. MODELING METHODS

Our proposed synthetic soft error rate simulation system covers individual transistors, primitive circuit cells, and micro-processor LSI chips. Figure 1 shows this simulation system flow. Firstly, individual MOSFET devices are analyzed by transient 3D device simulator ("HyDeleos" developed by SELETE [2]) by means of the pulse current response to the charged secondary-ion impacts.

Then, these current pulse wave-forms are utilized in the SPICE circuit simulation onto the primitive circuit cells for determining a SEU (single-event-upset) rate for FF or Latch sequential-type cells and propagation probabilities of the susceptible certain erroneous pulse width for any arithmetic combinational cells such as INV or NAND.

In our procedure, as shown in Fig. 2, a half of VDD is set to be a criteria of the erroneous pulse width (window-of-vulnerability), and the probability value causing this pulse width is searched by the iterative SPICE calculation of the primitive cell under different secondary ion striking events.

Once all the primitive circuit cells are characterized, large-scale integrated system chip FIT analyses are performed by the gate-level net-list analyzing tool "SoCFIT"[3]. The soft error failure rates, i.e. FIT values, are calculated as the following equations.

$$FIT = FIT_{seq} + FIT_{comb} + FIT_{mem} \quad (1)$$

$$FIT_{seq} = \sum \sigma_{seq} * LogicDR * TimeDR \quad (2)$$

$$FIT_{comb} = \sum \sigma_{comb} * LogicDR * TimeDR \quad (3)$$

$$FIT_{mem} = \sum \sigma_{mem} * Memory\_size \quad (4)$$

Here, FITseq, FITcomb and FITmem represent FIT values for the sequential-type circuit cells, the combinational cells and memory cells, respectively. σ represents the cross section value for the soft-error events of the cell. LogicDR and TimeDR represent the values for logical and time de-rating factors, respectively. Total FIT values on the chip-level are calculated as a sum of the components of sequential cell SEU and combinational cell SET FIT values (and FIT values from memory-blocks).

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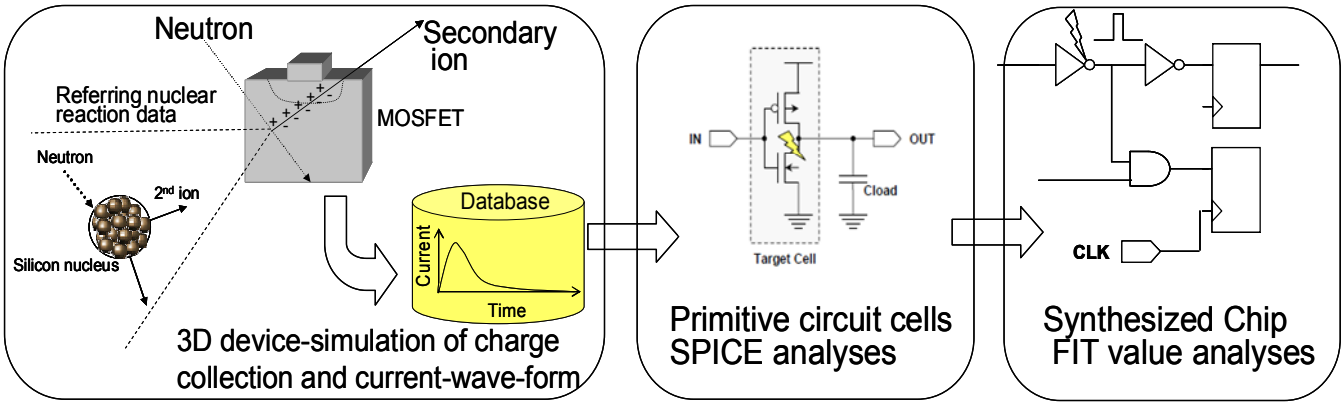

Figure 1. Constructed Simulation flow

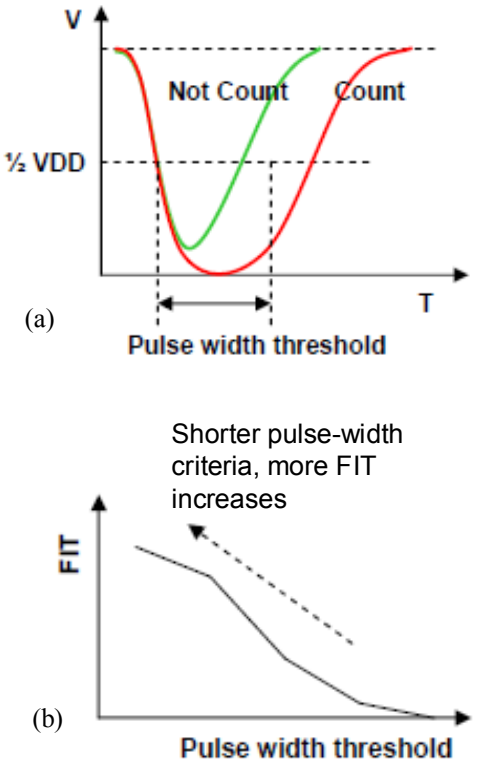

Figure 2. A procedure for the susceptible pulse width search for the primitive cells. By the iterative calculation, probability values causing the events crossing the specific pulse width threshold (a) are obtained as depicted in (b).

We have enhanced simulation efficiency tabulating transient 3D device-simulation results of many pulse current responses into a database table-file considering wide range of neutron-induced secondary ion striking events under some different applied voltage bias conditions.

"TFIT" [3-4] was used to carry out this procedure. This database is referred instead of the direct 3D device simulation of the current wave-form during the probabilistic search for the specific pulse width onto the primitive cells. We have confirmed this database table accuracy by the mixed-mode 3D device and SPICE combinational simulations (Fig.3-4) and observed more than 100 times CPU-time efficiency for the typical standard cells cases. Figures 3-4 show calculation results for a vertical ion incidence response onto an inverter cell performed by a mixed-mode circuit/device simulation and the TFIT simulation. The mixed-mode circuit/device simulation mentioned here represents that the SPICE circuit simulation with the nMOSFET in the inverter was replaced by 3D transient device simulation where the incident ion generates certain amount of the excess charge in the device body. Figure 3 shows the calculation results for the terminal-current pulse comparing the method based on the tabulated-device-simulation-data (using "TFIT") and 3D mixed-mode circuit-device simulation. Figure 4 shows the calculation results for the voltage drop after the ion incident event. These are almost identical for both current and voltage pulse shapes.

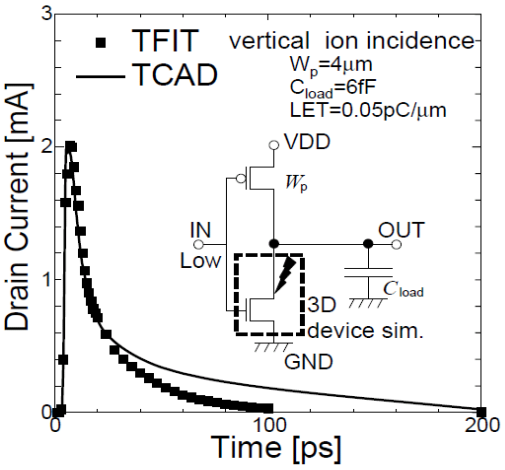

Figure 3. Comparison between the method based on the tabulated-device-simulation-data (using "TFIT") and 3D mixed-mode circuit-device simulation for the calculation of the current pulse curves.

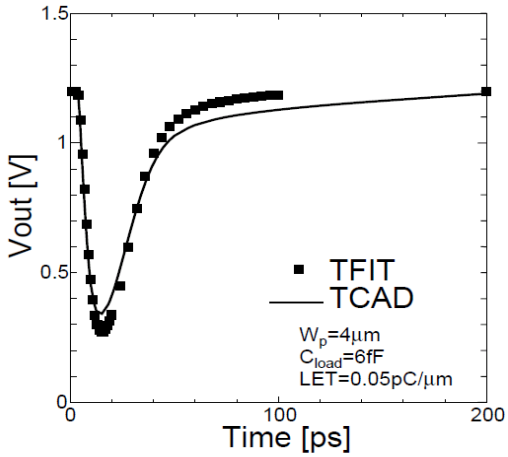

Figure 4. Comparison between the method based on the tabulated-device-simulation-data (using "TFIT") and 3D mixed-mode circuit-device simulation for the calculation of the transient voltage pulse curves.

III. Results and Discussion

Several kinds of primitive cells of 90nm technology generation have been characterized and we have found certain interesting features by means of the SET susceptibility which can be useful for the first-order approximated evaluation of the soft error impact on the different technology generation application and future prospect. Some of our findings are presented in Figs 5-6. Figure 5 shows the calculated event-causing probability for certain pulse-width threshold values for the typical standard cell library as indicated, referring commercial 90nm generation technology. In the Fig.5, roughly about three kinds of characteristic grouping can be seen depending on the cell-types.

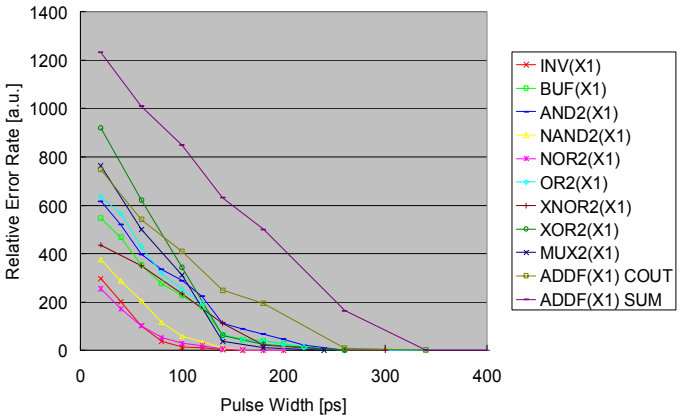

Figure 5. Calculated event-causing probability for certain pulse-width threshold values for the typical standard cell library as indicated, referring commercial 90nm generation technology.

Figure 6 shows the calculated SET probability values as a function of pulse width threshold values for the inverter (INV) cells having different driving capability. Plotted curves in the Fig. 6 indicate that the INV cells with high drivability tend to give high immunity for the pulse generation/transmission namely the SET. The inverter cell with a higher drivability tends to have a larger area of the diffusion layers which may be able to capture more secondary ion incident events. However, from the transient pulse (SET pulse) generation/transmission view point, the high drivability inverters tend to contribute fast recovery of the voltage drop caused by the excess charge from the secondary ion striking events, thereby show small rates as shown in Fig. 6.

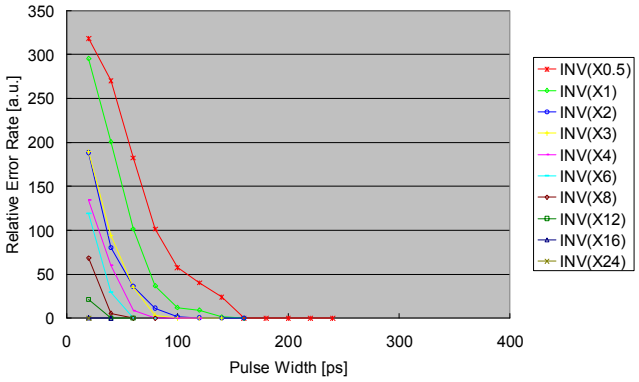

Fig. 6: Calculated SET probability as a function of pulse width threshold values. Inverters with high-drivability show small rates.

For the demonstration purpose, chip-level FIT calculations were performed onto the LEON2 32-bit processor [5] as the design of the processor is freely available under GPL license. The primitive results are summarized in Table 1.

Our simulation system helps us to understand certain influence of the SET phenomena versus SEU under different operational frequency.

Table 1. Example of the chip-level FIT simulation results, performed by using the gate-level net-list analyzing program called "SoCFIT"

Ope. Frequency	SEU (without memory)	SET (without memory)
Low	1	~0.01
High	~1	~0.1

IV. Conclusion

Soft error phenomena induced by the Sea-level cosmic neutron have been investigated by using a simulation system from individual MOSFET devices to LSI-chip level. A comprehensive practical simulation flow is demonstrated on commercial 90nm generation logic devices and standard-cells. This synthetic soft error rate simulation system enables us performing comprehensive analyses of SET phenomena on the different levels of the LSI technology: from the device to chip level, thereby becoming useful for further global design optimization.

Acknowledgments

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