Air-Spacer Self-Aligned Contact MOSFET for Future Dense Memories

Jemin Park and Chenming Hu
Department of Electrical Engineering and Computer Sciences,
University of California, Berkeley, CA 94720, USA
Tel: (510) 643-2637, Fax: (510) 643-2636, e-mail: jemins@eecs.berkeley.edu

I. ABSTRACT

An air-spacer SAC (Self-Aligned Contact) transistor is proposed. Air-spacer is created by removing the nitride spacer after the SAC plug has been formed. 3D mixed mode simulation shows that the 35% area benefit can be retained while improving the speed to be 10% better than a non-SAC device and switching energy to 82%.

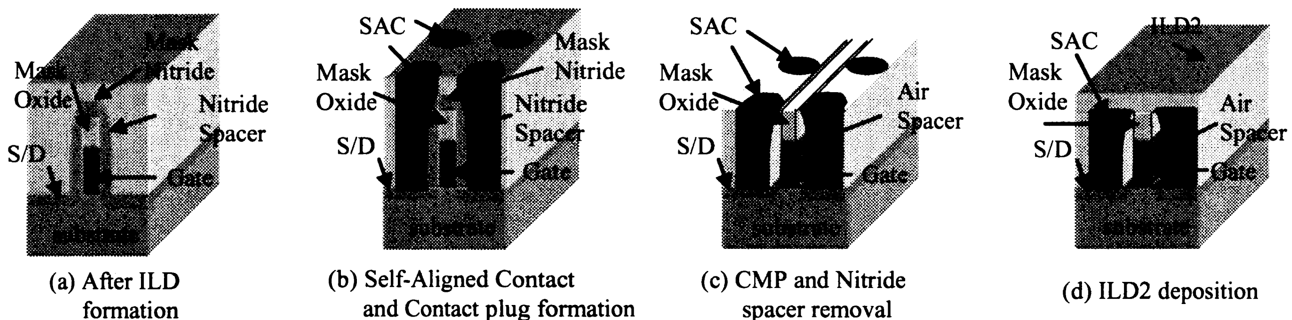
II. INTRODUCTION

At very small gate lengths, it is difficult to increase I_{DS}, and minimizing the capacitance takes on greater importance for speed with the added benefit of CV^2 reduction. At 20nm gate length, 77% of the gate charge is due to gate to contact-plug and to S/D diffusion capacitances with the rest attributable to capacitance to body and channel [1]. This fraction is even larger in dense memory devices because the SAC technology places the contact plug closer to the gate and the spacer material is nitride having nearly twice the k of SiO_2. Giving up the SAC technology will of course improve the gate capacitance but the sacrifice in density would be unacceptable. It will be critical to reduce the gate to SAC capacitance in order to reduce the device, bit-line, and world-line capacitances for better speed and power.

We propose a novel air-spacer transistor that does not sacrifice the SAC density and reduces the gate capacitance, power, and delay to levels even lower than conventional non-SAC transistor. With this combination of density and performance, air-spacer SAC transistor could be attractive to not only DRAM (Dynamic Random Array Memory), but also to SRAM (Static Random Array Memory), embedded SRAM, and perhaps even other applications. While Togo reported only 6% speed improvement in 0.25μm air-spacer non-SAC transistors [2], this paper investigates the potentially much larger improvement in 22nm SAC devices.

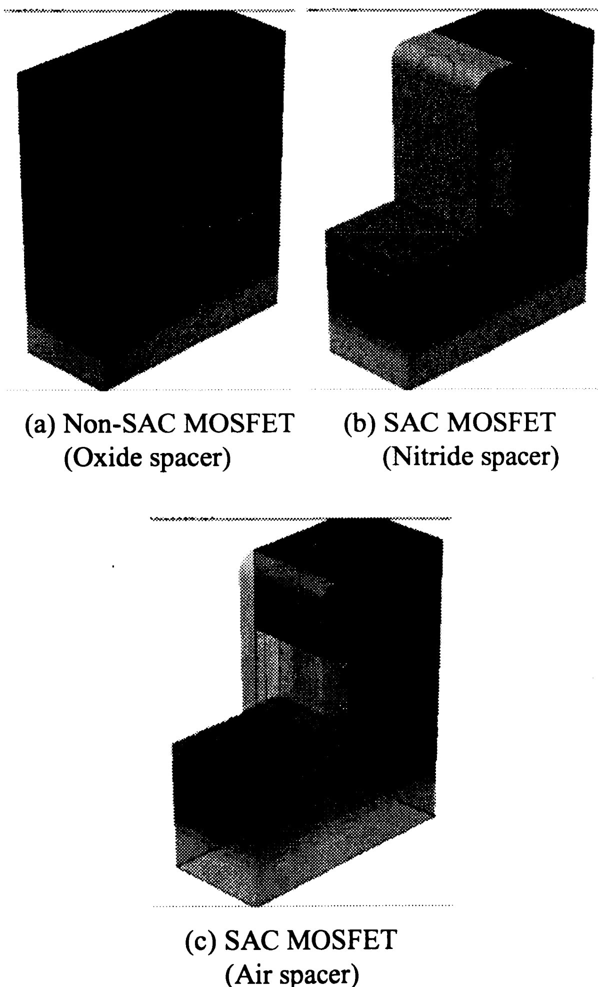
III. CONCEPT AND PROCESS SIMULATION

The proposed air-spacer process flow is as follows. In Figure 1(a), mask nitride/oxide and gate have been patterned, nitride spacer and S/D



(a) After ILD formation (b) Self-Aligned Contact and Contact plug formation (c) CMP and Nitride spacer removal (d) ILD2 deposition

Figure 1: Proposed process flow of the novel air-spacer SAC transistor.


(a) Non-SAC MOSFET (Oxide spacer) (b) SAC MOSFET (Nitride spacer)

(c) SAC MOSFET (Air spacer)

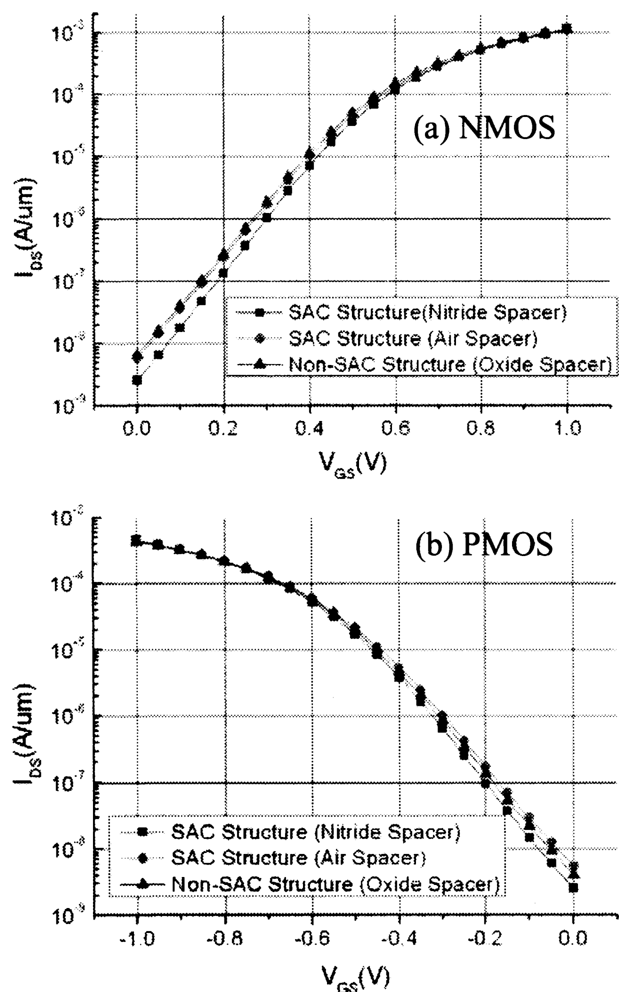


Figure 2: MOSFETs constructed with 3D simulator. In (b) (c) part of ILD is removed to show the outlines of SAC. Lgate = 20nm, nitride/oxide/air spacer thickness= 12nm.

Figure 3: Simulated I-V characteristics of the MOSFETs are basically the same.

formed, ILD (Inter-Layer Dielectric) deposited, and oxide CMP (Chemical Mechanical Polishing) carried out. Figure 1(b) shows that SAC has been formed by high-selectivity contact hole etch and contact plug filling. Excess plug material over the surface is not shown. Figure 1(c) shows the novel steps of CMP to expose the top of the mask nitride and selective etch of the nitride mask/spacer without etching the oxide to create an air gap. A very thin oxide liner is deposited underneath the nitride spacer to protect the gate dielectric from this etch step. Figure 1(d) shows non-conformal ILD2 deposition has sealed the top openings and completed the air spacers.

3D Computer simulations were performed. First we constructed the transistors using 2D TSUPREM-4 [3]. From that we constructed 3D structures with contacts using the Sentaurus structure editor [4]. We compared three devices: conventional non-SAC device in Figure 2(a), conventional SAC device in Figure 2(b), and the new air-spacer SAC device in Figure 2(c). Except for the spacer and contact, the three transistors have identical design parameters such as Source / Drain

and channel doping, T_{ox}, and L_{gate}. In order to suppress the short channel effect, retrograde body doping is created with a 500 Å 2e18/cm^3 doped region and a 210 Å 1e16/cm^3 doped epitaxial layer at the surface. Gate oxide thickness is 1.5nm. The gate length is 20nm and the thickness of the gate is 600 Å. The thickness of all three types of spacer is 12nm. In the case of the non-SAC device, the spacing between gate and contact is 30nm. The three PMOSFETs are the same as the NMOSFETs except for the doping.

IV. DEVICE SIMULATION RESULTS

The characteristics of transistors and inverters are simulated with Sentaurus 3D device simulator [4]. Figure 3 shows that the I_{DS}-V_{GS} characteristics of the three transistors are little changed by the spacer/contact designs. There are all the same channel and source/drain implants because of fairly comparing the characteristics among 3 different transistors. There will be no change of I_{DS}-V_{GS} characteristics if we optimize the channel and source/drain doping in both 2D and 3D simulation.

Figure 4 shows a schematic of the inverter chains that were simulated with 3D mixed–mode simulation. The NMOSFETs have 70nm width channel and the PMOSFETs, 140nm width channel. The input voltage ramps up at t=1E-11s and back down at 8E-11s as shown in Figure 4. The inverter delay is defined by the average of the pull-up and pull-down delays measured at 50% V_{DD}. The delays can be read in Table I. The conventional non-SAC inverter has 10% longer delay than the air-spacer SAC inverter; the conventional SAC inverter, with nitride spacers, 78%. Similar benefits were observed for air-spacer SAC transistors in terms of switching energy or switching charge/capacitance as shown in Table I.

Figure 5 illustrates the density advantage of SAC devices over non-SAC devices. The area difference is shown in the bottom row of Table 1.

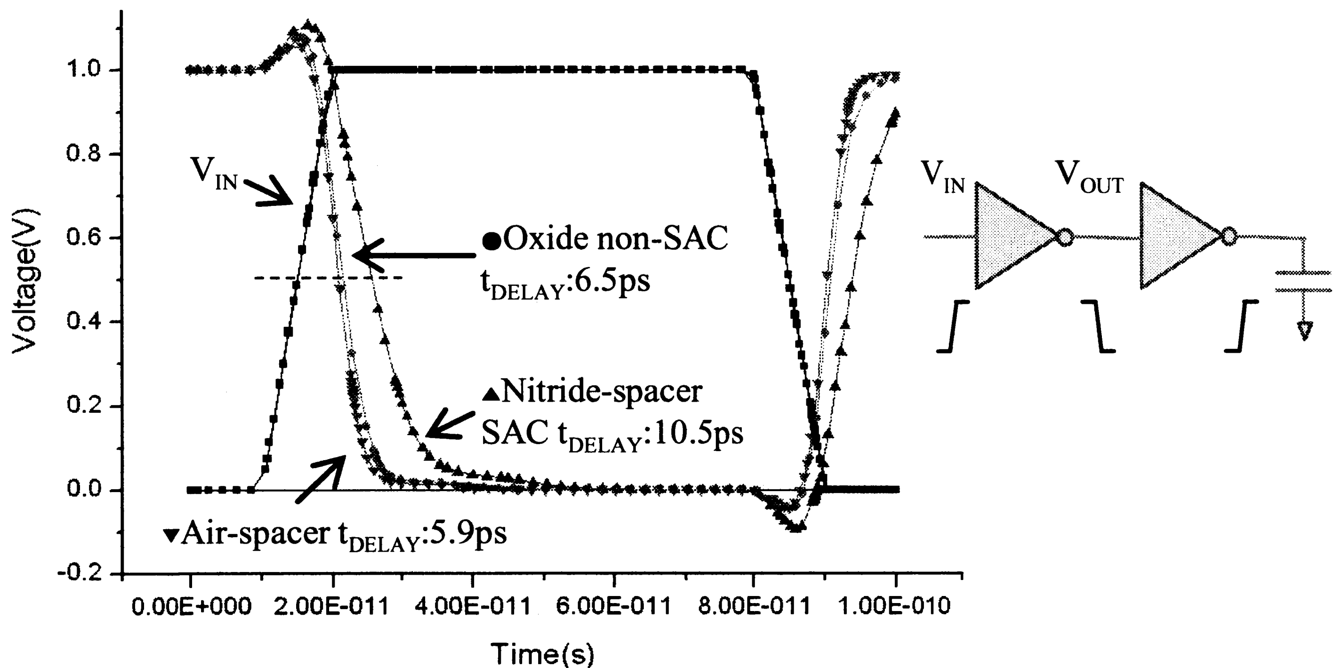


Figure 4: Mixed-mode simulated delay of air-spacer inverter is 9% and 46% smaller than nitride-spacer and non-SAC cases.

Table I: Summary of comparison. Bottom three rows show air-spacer SAC to excel in speed, switch energy/capacitance, and area.

	Non-SAC Oxide Spacer	SAC Nitride Spacer	SAC Air Spacer
NMOS ION/IOFF (A/μm)	1.11e-3 / 6.55e-9	1.13e-3 / 2.56e-9	1.08e-3 / 5.74e-9
PMOS ION/IOFF (A/μm)	4.32e-4 / 4.03e-9	4.51e-4 / 2.53e-9	4.40e-4 / 5.50e-9
Inverter Delay (ps)	6.5	10.5	5.9
Delay relative to Air-spacer SAC	1.10	1.78	1
Switching Charge relative to Air-spacer SAC	1.30	2.56	1
Switching Energy/Capacitance relative to Air-spacer SAC	1.22	2.51	1
Area relative to Air-spacer SAC	1.5	1	1

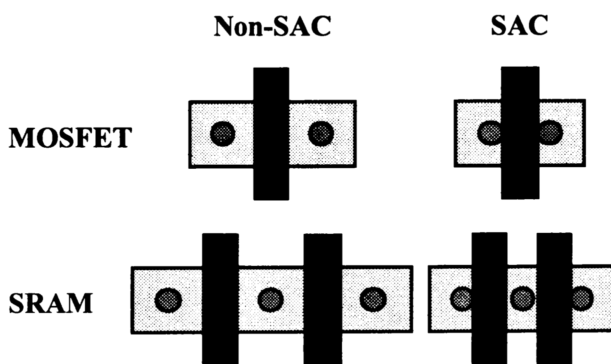


Figure 5: Area comparison of non-SAC and SAC MOSFET and SRAM.

V. CONCLUSION

Reducing the device capacitance will be an increasingly important way to improve the device speed and switching energy/power at 22nm and beyond. High density memories employ the SAC technology that requires the use of nitride spacers. This significantly raises the gate to plug/diffusion capacitance and increases the delay and switching energy by over 60% and 100%, respectively. A novel air-spacer SAC device can preserve the 35% area benefit of SAC device while reducing the delay and power by about 10% and 18% respectively, to levels even better than the non-SAC conventional device. It also reduces the bit-line and word-line capacitances. The result is increased DRAM and SRAM speed, reduced power, and reduced chip size.

REFERENCES

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