2D Simulation of Gate Currents in MOSFETs: Comparison between *S-Device* and the Quantum Mechanical Simulator *GreenSolver*

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***Abstract*—The gate leakage current caused by direct tunneling in a double-gate n-type MOSFET with a physical gate length of 22 nm is studied. Two approaches are compared: a one-dimensional (1D) Schrödinger-Poisson solver coupled to the common drift-diffusion model and a two-dimensional (2D), full quantum mechanical computation of the current. In the first approach, the tunnel probability through the gate dielectric is obtained on straight lines that connect points in the channel with the gate. The second method uses a 2D Schrödinger-Poisson solver with open boundary conditions where carriers are injected from the source, drain, and gate terminals. The dielectric layer has an equivalent oxide thickness of 1.2 nm and is either composed of pure SiO_2 or of a high-K SiO_x-HfO_2 stack. It is found that the leakage currents calculated with the 2D approach are significantly larger due to diffraction of the electron waves at both edges of the gate contact.**

I. INTRODUCTION

High dielectric constant ("high-K") materials, such as HfO_2, have now reached the stage where they are used in gate stacks of silicon based MOSFET's [1]. The HfO_2 insulator comes along with metal gate electrodes and a thin (typically $\leq$ 10 Å) inter-facial SiO_x or oxynitride layer. Modeling the leakage currents in metal-gate/HfO_2/SiO_x/Si structures requires knowledge of the dominant conduction mechanism and the physical parameters (permittivities, band offsets, effective tunneling masses), the latter being crucial for meaningful TCAD applications. Based on an n-type double-gate transistor designed to fulfill the requirements of the 22 nm technology node [2], we apply two tunneling models with different complexity and computational burden. Whereas the first model relies on the solution of the conventional 1D Schrödinger-Poisson system, the second, more evolved model uses a 2D and real-space Schrödinger-Poisson solver with open boundary conditions at all terminals. Such a model is capable to describe the increase of tunneling leakage due to electron diffraction at the gate corners.

II. SIMULATION APPROACHES

In the conventional approach (S-Device), 1D Schrödinger equations are solved along straight lines connecting the channel to the gate contact [3], [4]. The gate current is self-consistently coupled to the drift-diffusion transport model. A special-purpose grid is defined which consists of lines that are attached to a semiconductor vertex and connect this vertex to the closest grid point on the gate contact. Also points not directly situated under the gate can be connected to the gate corners by defining a maximum angle measured to the normal of the gate contact line. All data on the initial grid are interpolated to the special-purpose grid. The 1D Schrödinger equation is solved in the (one-band) effective mass approximation (EMA) using the scattering matrix approach [5].

The 2D approach (GreenSolver package) treats the device and the gate contact as a single entity on a quantum mechanical level. To allow electrons to enter and exit the simulation domain at the source, drain, and gate contacts, a real-space Schrödinger-Poisson solver has to be used instead of the popular mode-space approximation which separates the longitudinal and transverse directions [7], [8]. The simulation domain is discretized by the finite difference method. The z-direction is assumed periodic and induces a k_z-dependence that modifies the injection probability of the electrons [8]. At all contacts a single-band scattering boundary ansatz [9], [10] is applied to model the open boundary conditions (OBC). Working in the EMA Wave Function (WF) formalism instead of the Non-Equilibrium Green's Function formalism ensures that all elements of the gate boundary self-energy Σ_G can easily be taken into account. In the NEGF approach proposed in Ref. [11] or [12] only the first off-diagonal blocks of Σ_G are kept, and the higher-order elements are neglected. The consequences of this omission have not been explored yet. In the WF formalism the Schrödinger equation has the following form:

$$\underbrace{(\mathbf{E}-\mathbf{H}-\mathbf{\Sigma_S}-\mathbf{\Sigma_D}-\mathbf{\Sigma_G})}_{\mathbf{A}}\cdot\phi = \mathbf{S_{inj}}. \quad (1)$$

The variable ϕ represents the wave function at each discretization point in the device. The matrices $\mathbf{\Sigma_S}$ and $\mathbf{\Sigma_D}$ model the injection mechanism from the source and drain contacts and vanish everywhere except in the left and right corner of $\mathbf{A}$, $\mathbf{\Sigma_G}$

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occupies a large sparse block in the middle of $\mathbf{A}$ and destroys its block tri-diagonal structure inherited from $\mathbf{H}$ [11]. The N_{S} states injected from the source, N_{D} from the drain, and N_{G} from the gate are included in the $(N_{\mathrm{S}} \cdot N_{\mathrm{D}} \cdot N_{\mathrm{G}}) \times (N_{\mathrm{x}} \cdot N_{\mathrm{y}})$ matrix $\mathbf{S_{inj}}$.

The linear system (1) is solved with a direct sparse linear solver [10] for each injection energy E and for the six degenerate conduction band valleys of Si. On a non-uniform finite difference grid the matrix $\mathbf{A}$ is not symmetric, but it can be symmetrized by a basis transformation [13], which then simplifies the factorization of $\mathbf{A}$. The advantages of working in the Wave Function formalism as in Eq. (1) over Non-Equilibrium Green's Functions (NEGF) are (a) a better numerical efficiency [14] and (b) a more accurate physical description as explained above.

III. Device description

The structure of the 22 nm nMOSFET was originally designed in the framework of the European project PULLNANO [15] as double-gate architecture. It is symmetrical with respect to the center of the channel (see Fig. 1). The geometry has

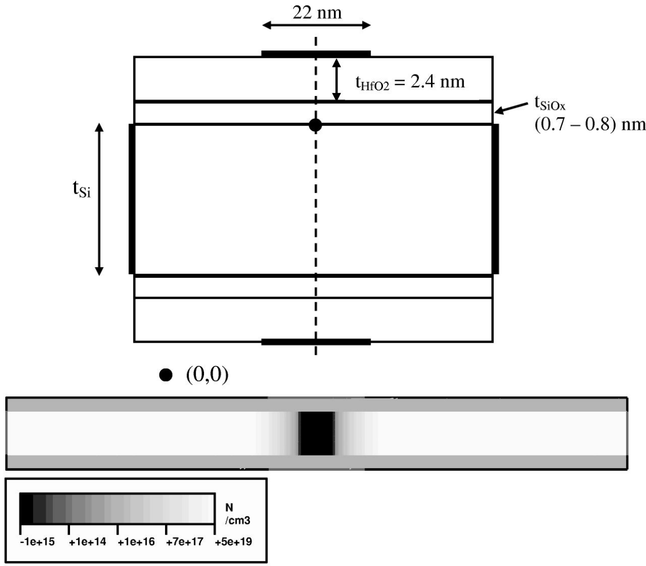

Fig. 1. Upper: Schematic of the 22 nm double-gate SOI transistor. Lower: Geometry and doping profile.

been slightly changed for the purpose of this paper (e.g. shorter source/drain regions). Here, the high-K gate stack consists of a 0.8 nm inter-facial SiO_x layer and 2.4 nm of $\mathrm{HfO_2}$. The gate length is 22 nm, the channel is unstrained with $\langle 100 \rangle$ orientation, the body thickness is 10 nm, the source/drain extensions are 20 nm long in all simulations, and the contacts are placed vertically at the ends of these extensions. Structure and doping information were translated into S-Device input files by the PULLNANO consortium. The material parameters for the effective mass framework were determined by extensive comparisons of measured and simulated CV and gate current characteristics of various kinds of capacitors and MOSFETs. As a best compromise the following set of parameters was identified and used in this paper: gate work function = 4.6 eV, $\epsilon_{\mathrm{HfO2}} = 23$, $\epsilon_{\mathrm{SiO2}} = 3.9$, $\chi_{\mathrm{HfO2}} = 2.05\,\mathrm{eV}$, $\mathrm{m_{HfO2}} = 0.11\,\mathrm{m_0}$, $\chi_{\mathrm{SiO2}} = 0.9\,\mathrm{eV}$, $\mathrm{m_{SiO2}} = 0.5\,\mathrm{m_0}$.

IV. Results

Fig. 2 shows the drain and gate current characteristics at $\mathrm{V_{DS}}$ = 1 V as obtained with S-Device including (non-local) band-to-band (B2B) tunneling in the drain-body junction. In this simulation the interlayer thickness was t_{SiOx} = 0.7 nm (anywhere else t_{SiOx} = 0.8 nm). It can be seen that in the GIDL range the direct gate tunneling current is influenced by the B2B

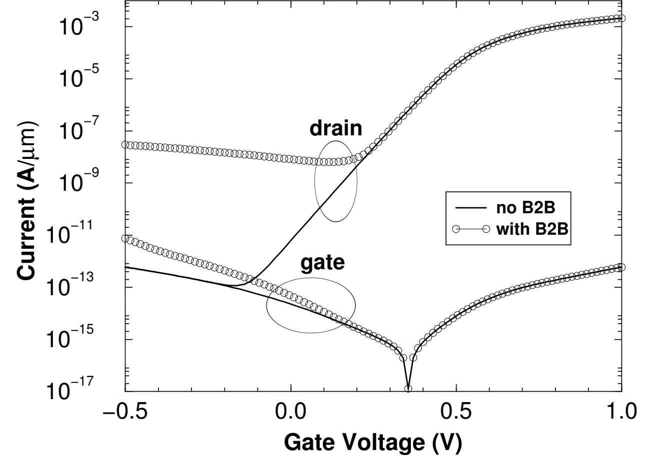

Fig. 2. Drain and gate current characteristics from S-Device at $\mathrm{V_{DS}}$ = 1 V.

generation. In the further analysis B2B was neglected. The 2D gate tunneling simulation reveals that the gate current paths have the form of curved lines which describe the diffraction of the electron wave (Fig. 3). Despite the fact that such a tunneling path has a lower probability than the corresponding

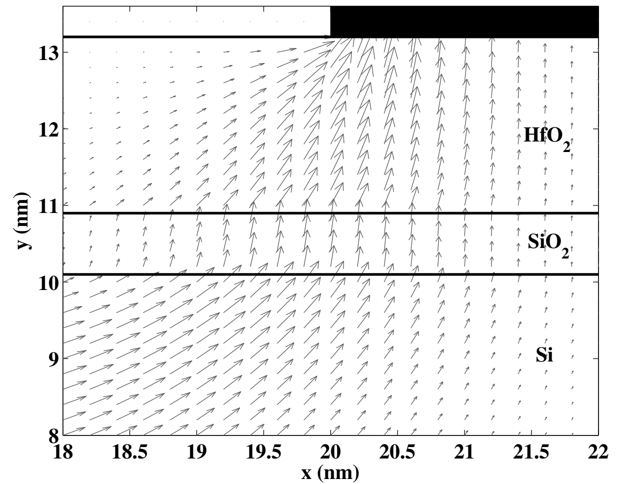

Fig. 3. Electron trajectories at the gate corner from the 2D quantum-ballistic simulation for $\mathrm{V_{DS}}$ = 0 V and $\mathrm{V_{GS}}$ = 0.1 V.

straight path to the gate, it induces more leakage current since more carriers are available due to the higher doping level at the starting point. A 2D quantum transport simulator fully accounts for this effect, while 1D wave functions along straight lines are unsuited to obtain such trajectories. The effect on the gate current is shown in Fig. 4 for V_{DS} = 0.1 V and in Fig. 5 for V_{DS} = 1.0 V. The full 2D quantum mechanical simulator

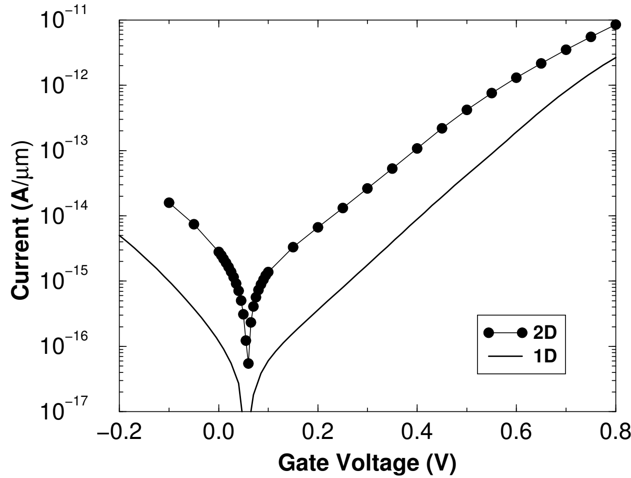

Fig. 4. Gate current characteristics from the two models at V_{DS} = 0.1 V.

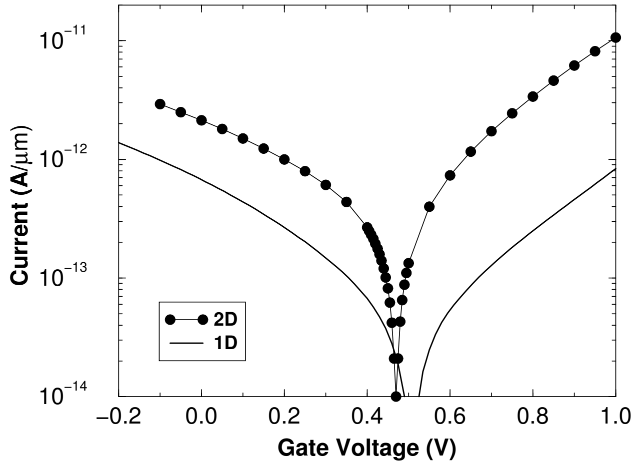

Fig. 5. Gate current characteristics from the two models at V_{DS} = 1.0 V.

exhibits a gate current that can exceed 10 times the current from 1D approach depending on the gate voltage. Fig. 6 shows the suppression of gate leakage when a pure SiO_2 layer with the same EOT is replaced by the SiO_x-HfO_2 gate stack. This suppression amounts to factors 212 (1D) and 810 (2D) for the on-state and to factors 2167 (1D) and 4546 (2D) for the off-state. The corresponding transfer characteristics are shown in Fig. 7. For the off-state there is no difference in the case with high-K stack (drain current not influenced by the gate current), but a factor 6 difference in the case of pure SiO_2 layer with the same EOT. This is of course based an the assumption that the gate work function is 4.6 eV.

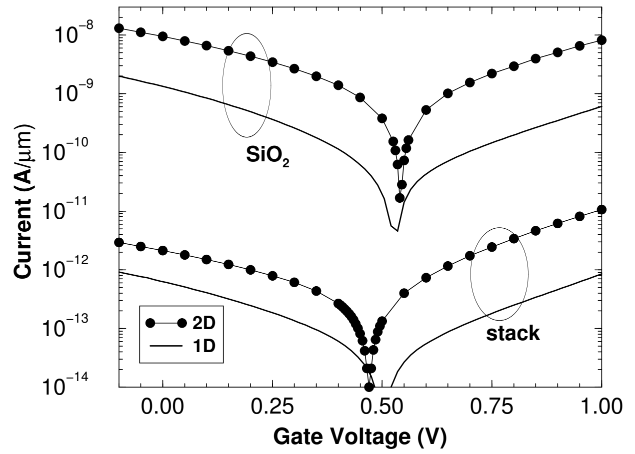

Fig. 6. Gate current characteristics from the two models at V_{DS} = 1.0 V with the SiO_2-HfO_2 gate stack replaced by pure SiO_2 with the same EOT.

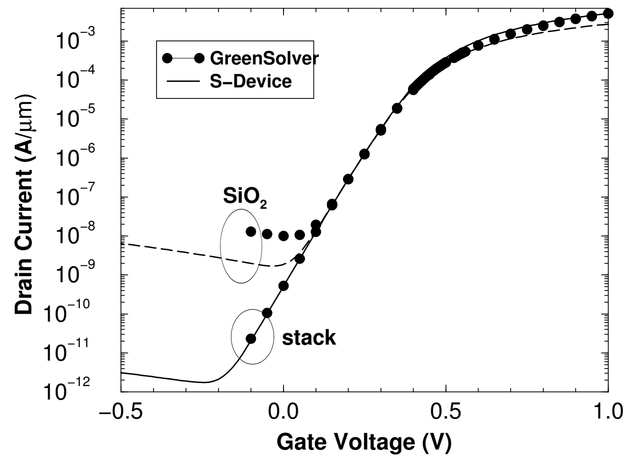

Fig. 7. Transfer characteristics at V_{DS} = 1.0 V for SiO_2-HfO_2 and pure SiO_2 dielectric, respectively.

V. CONCLUSION

The gate currents of a 22 nm n-type double-gate transistor with either a single SiO_2 dielectric or a high-K gate stack were studied by two different methods, a 1D approach incorporated in the drift-diffusion simulator S-Device, and a 2D and real-space Schrödinger-Poisson solver. The 1D treatment always underestimates the gate current because it fails to include the important effect of electron diffraction at the gate corners. In the case of out-tunneling (low drain bias), the difference mainly comes from curved trajectories that have their starting points outside the gate region. Here, due to the lateral doping profile, the carrier density is much higher than directly under the gate. This electron diffraction, completely absent in the 1D approach, gives about 20 times more current at low gate voltages. Only at very large gate voltages (and low drain bias) both methods converge. The actual OFF-state leakage is determined by in-tunneling electrons in a narrow interval ($<$ 2 nm) at the drain-side gate corners. Also here, the 1D approach underestimates the OFF-current for both gate di-

electrics. Curved trajectories are advantageous leakage paths since at their end points the band edge is at a lower energy compared to points directly under the gate and, therefore, the carrier velocity is larger there. The reason for this effect is the rapid voltage drop in the pinch-off region. For the 22 nm double-gate FET this increases the OFF-current by a factor of 3.3 for the high-K gate stack and by a factor of 7.1 for pure SiO_2 dielectric. One can conclude that for the design of future high-K stack configurations a 2D and full quantum mechanical treatment of gate leakage should be envisaged.

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