Operational PRAM Analysis with PVT Variations Using Process-aware Compact Model

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Abstract – **In this paper, we present for the first time a process-aware compact model to describe cell characteristics of PRAM. Applying this model, we have performed hierarchical sensitivity analysis on the process, voltage, and temperature (PVT) variations and studied impacts on the sensing margin.**

Keywords-PRAM; phase change; variation; compact model; simulation.

I. INTRODUCTION

The phase change random access memory (PRAM) has emerged as the most promising device for high density products among various nonvolatile memory devices. However, low power operation as a key issue for high density products has mainly depended on cell size scaling. Process variations become one of the major concerns for PRAM scaling, as shown in Fig. 1 [1]. Thus, the variation tolerant design based on statistical methodology is required at the development stage. Although recent studies have provided basic understandings on the operational principles and reliability issues [2], the simulation methodology on aspects of process variations has not been proposed. Moreover, the separation of variation components through sensitivity analysis has not been performed due to the limitation of describing cell characteristics. In this study, we propose a process-aware compact model considering phase-change mechanism. Applying this model, sensitivity analysis on various PVT variations is performed, with taking all of cell and core/periphery circuits into account.

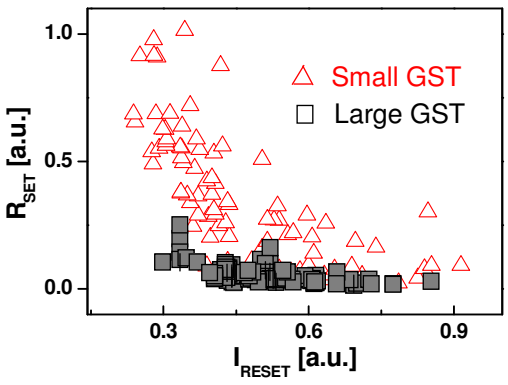

Figure 1. Resistance distributions for two different GST size.

II. PHYSICAL-BASED OPERATIONAL MODELING

An overall simulation flow is designed to span whole hierarchy from the device modeling of GST cell to the full-chip circuit analysis, as shown in Fig. 2. It seamlessly proceeds through pre- and main- processes and the essence is the analytic model for electro-thermal/phase-change simulation in Fig. 3(a) [3,4] and the compact circuit model. Correlation of numerical and experimental results on key electrical quantities of cell (R_{SET}, R_{RESET}, V_{TH}, and V_H), with taking process and voltage variations into account, are represented in analytic forms via the RSM modeling, as shown in Fig. 3(a). The electrical parameters are formulated as functions of process and input-pulse variables, and then the interface between the device-level analysis and the compact model is explicitly defined, as shown in Fig. 3(b).

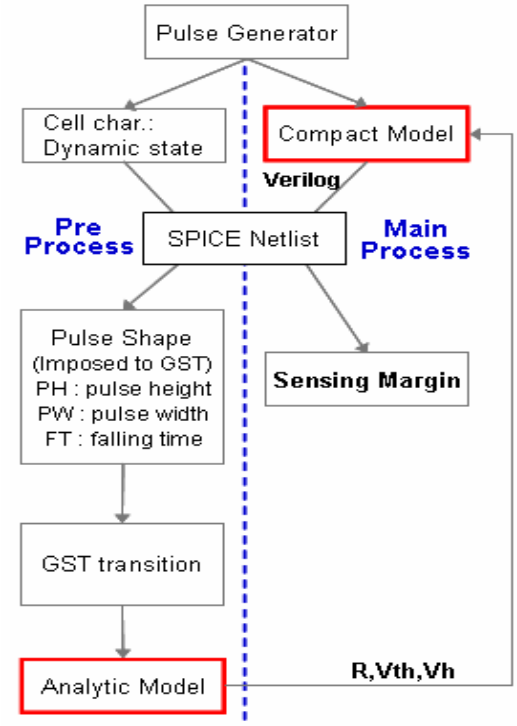

Figure 2. Simulation flow for analyzing sensing margin

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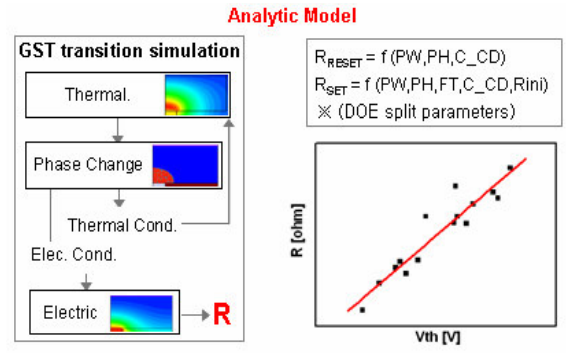
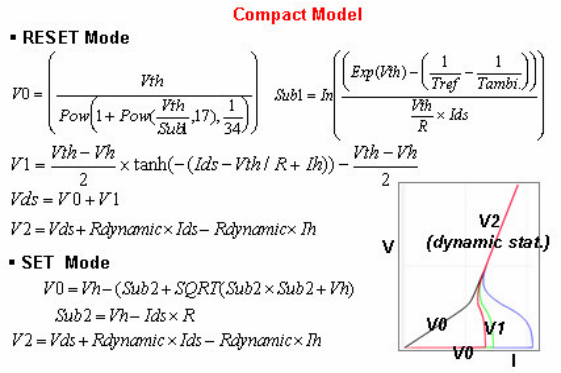


(a)



(b)

Figure 3. Proposed analytic and compact model. (a) GST transition is implemented through the thermal, phase change and electric simulations, orderly. Resistance and Vth are obtained by numerical and empirical simulation. (b) Compact model consist of four types of equation; SET state describes V0 and V2, while RESET state describes V0,V1 and V2. Holding current and the current imposed to GST are described by Ih and Ids, respectively.

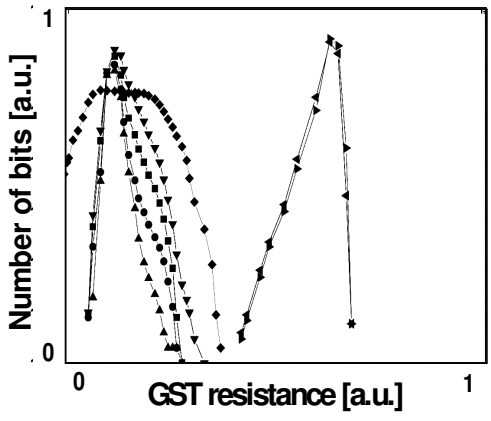


Figure 4. Resistance distributions after RESET and SET operation with various duration conditions.

With given operational conditions and process/voltage variation, the programming pulse imposed to GST cell is determined with the pre-processing circuit simulation and the cell resistances and the threshold/holding voltages in compact model are determined with analytic equations. Finally, the programming and the subsequent sensing operations are simulated with the main full-chip simulation and the operational margin is estimated in a self-consistent manner.

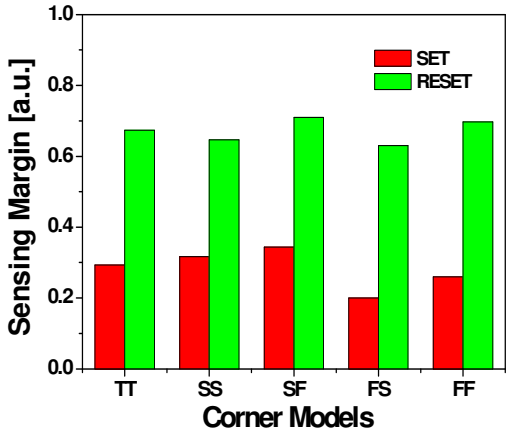


Figure 5. Sensing margin according to applying corner model. SET state is more sensitive.

III. SENSING MARGIN ANALYSIS

We analyze the sensing margin for PVT variations from resistance distributions of SET and RESET states in Fig. 4. Sensing margin is defined as voltage difference obtained from the proposed simulation flow. And, the sensitivity is analyzed by applying PVT variations at reference condition as follows.

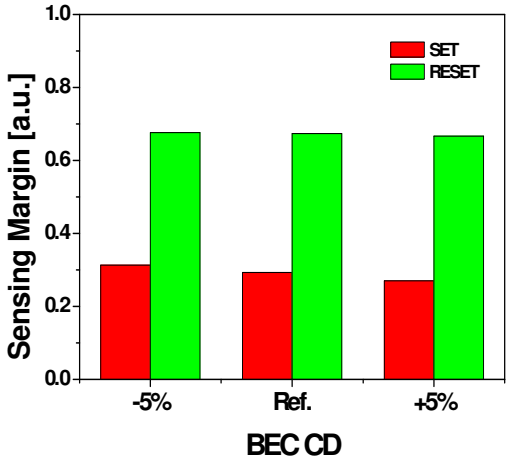


Figure 6. Bottom Electrode contact (BEC) size dependency of sensing margin.

A. Process variations

Process variation is classified into components in core/ periphery circuit and GST cell[5]. Sensing margin of core/periphery is obtained with simulation using ET-based corner models as shown in Fig. 5. The sensing margin is determined by SET resistance distribution since the SET state is more sensitive to the process variation. Therefore, an optimization of SET operation is required to secure the immunity to process variation. As Fig. 6 shows the effect of cell component, which is estimated by considering only the most sensitive bottom electrode contact (BEC) scaling, the BEC dependency for sensing margin is insignificant. In other words, the programming condition applied by this simulation is optimized.

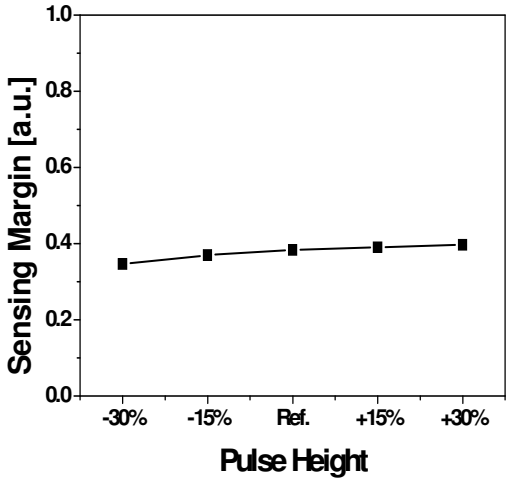


Figure 7. RESET pulse height dependency of sensing margin at constant SET condition.

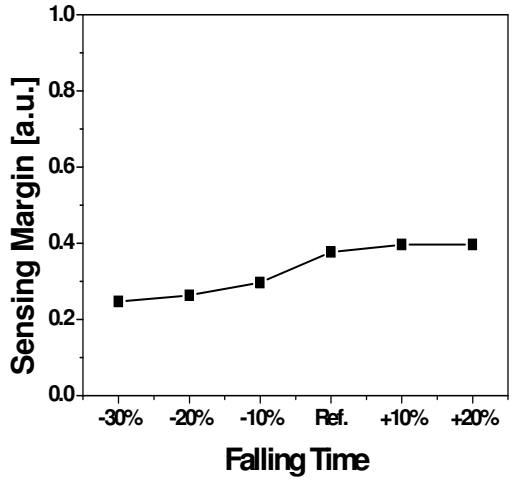


Figure 8. Falling time dependency of sensing margin at constant RESET condition. Falling time is very sensitive factor.

B. Voltage variation

Voltage variation is defined the characteristic of external circuit and all of parasitic components as pulse shapes. The dependence to the programming pulse, which consists mainly of pulse height and falling time, is analyzed in optimization point of view. Increasing pulse height and falling time improves sensing margin since the amorphization and crystallization of GST material are accelerated, as shown in Fig. 7 and 8. These results indicate a possibility of reducing the programming time as well as improving sensing margin by applying different pulses in SET and RESET operations, as shown in Fig. 9.

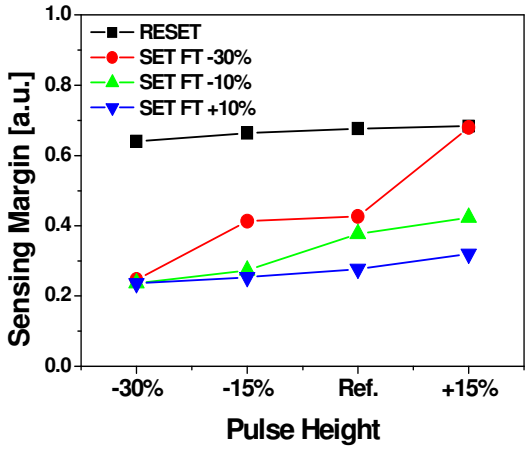


Figure 9. Pulse height and falling time dependency of sensing margin.

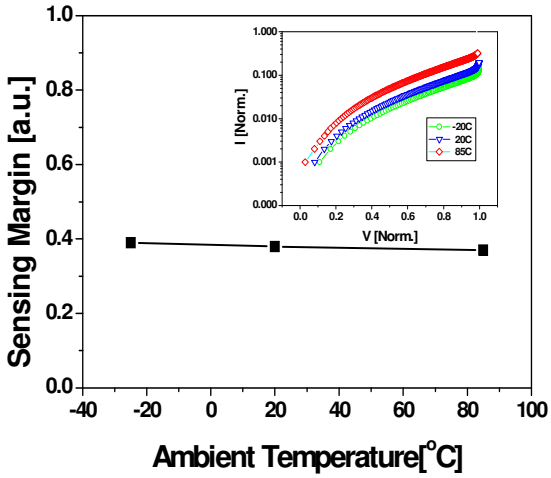


Figure 10. Ambient temperature dependency of sensing margin. I-V characteristics describes the effect of ambient temperature.

C. Temperature variation

The effect of ambient temperature is only considered at read operation in cell since write operation is implemented above about 200°C[6]. The sensing margin

changes little as the ambient temperature increases, as shown in Fig. 10. From these results, we can analogize that these simulations are carried out at stable RESET state.

IV. CONCLUSIONS

We have performed the hierarchical sensitivity analysis of sensing margin to PVT variations by applying physics-based process-aware compact model. From the analyses, the sensitivity of process and design control factors is defined.

V. REFERENCES

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