Study on the Optimized Design of Nanowire Tunneling Transistors Including Quantum Effects

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***Abstract*—To reduce shortchannel effects in modern nanoscale MOS devices alternative device concepts like the tunneling field effect transistor have been suggested. Since the complete current is sustained by tunneling processes, these devices obey different design rules than MOSFETs. Similarly, the use of multigate structures is an interesting approach to cope with undesired shortchannel effects. A very promising idea is the combination of these two concepts. Using physical device simulation, we investigate the functionality and performance of such nanowire tunneling transistors. Special attention is focussed on the possibility to improve the device performance by considering alternative materials for the gate-stack and the source region.**

I. INTRODUCTION

The progressive shrinking of the physical gate length of MOS-devices leads to a number of undesired shortchannel effects like punch-through, drain-induced barrier lowering (DIBL) and roll-off. Multigate structures are one promising concept to overcome these effects without a significant loss in performance. An alternative approach to tackling short channel effects exploits the idea of the tunneling field effect transistor (TFET) [1]. Here, tunneling is not an undesired parasitic effect, but constitutes the working principle. In previous work we studied the operation of such structures using numerical device simulation [2], [3] and came to the conclusion that the combination of the TFET with the multigate concept may be an attractive further option. This motivated us to investigate in detail the operational behavior of a cylindrical nanowire tunneling transistor and the effect of quantum confinement on its characteristics, with the focus on the optimization and the scalability of such devices. Among others, we studied potential device improvements by considering alternative materials for the gate-stack and the source region. So, for instance, we analyzed the influence of different gate metallizations and gate oxide materials. Additionally, we investigated the possibilities that emerge by the use of SiGe in the source region.

II. MODELING

Band-to-band tunneling and quantum confinement effects at the Si/SiO_2-interface under the gate essentially determine the device characteristics and, hence, must be properly included in the physical models used for simulation.

A. Density gradient model

A quasi-classical treatment of nanometer devices can be justified by introducing an additional quantum-potential as quantum-mechanical correction of the quasi-Fermi levels. The density gradient model is based on the assumption that Bohm's potential [5] may be written as

$$\Lambda = -\frac{\gamma \hbar^2}{6m^\star \sqrt{n}} \nabla^2 \sqrt{n} \qquad (1)$$

where the empirical parameter γ accounts for the relative occupancy of the different subbands. The electron density is then given by

$$n = N_c \cdot \exp\left(\frac{E_{Fn} - E_c - \Lambda}{kT}\right) \qquad (2)$$

where N_c is the conduction band density of states and E_c is the position-dependent conduction band edge. Combining both expressions yields an equation for $\sqrt{n}$, which has to be self-consistently solved together with the Poisson equation.

B. Phonon-assisted tunneling

Tunneling currents between strongly tilted energy bands are implemented in the drift-diffusion-like transport model by adding equivalent generation rates to the carrier source terms in the balance equations which represent the generation of electron-hole pairs in the middle of the bandgap.

Phonon-assisted tunneling is modeled on the basis of the Kubo formalism for the tunneling conductivity [7]. With the particle energy E and the electric field F this approach results in the sum of two generation rates of the form

$$G_{pat} = B \cdot |F|^\alpha \cdot D(F, E) \cdot \exp\left[-\frac{F_0}{|F|}\right] \qquad (3)$$

where $\alpha = 7/2$ holds for indirect semiconductor materials like silicon and $D = f_v - f_c$ denotes the Fermi-Dirac distribution functions related to the difference of intrinsic energy and the corresponding Fermi energy-levels. For numerical simulation this expression is re-written as

$$D = f_v - f_c = \frac{n_i^2 - np}{(n + n_i) \cdot (p + n_i)} \qquad (4)$$

C. Defect-assisted tunneling

A realistic physical model for tunneling via traps in the bandgap can be obtained from the effective-mass Schrödinger

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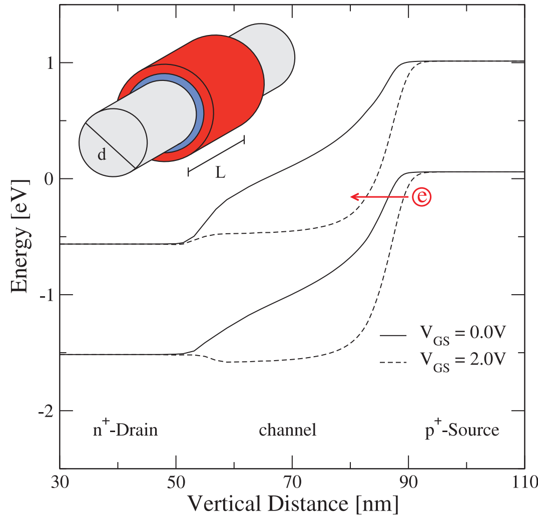

Fig. 1. Band diagram of the nanowire TFET at $V_{DS} = 0.5V$.

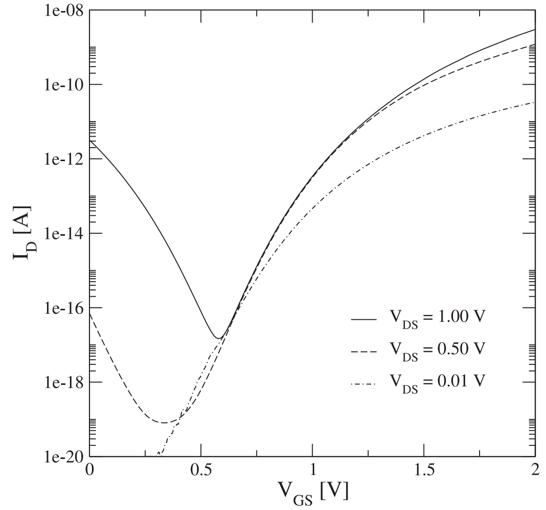

Fig. 2. Simulated transfer characteristics in n-operation mode.

equation under the assumption of a linear potential [8]. This leads to a Shockley-Read-Hall-like generation rate

$$G_{dat} = \frac{n_i^2 - np}{\frac{\tau_p}{\Gamma_p + 1}(n + n_1) + \frac{\tau_n}{\Gamma_n + 1}(p + p_1)} \tag{5}$$

where τ_n and τ_p denote recombination lifetimes of electrons and holes, and $\Gamma_{n,p}$ are field-dependent functions:

$$\Gamma_{n,p} = \frac{\Delta E_{n,p}}{kT} \cdot \int_0^1 \exp\left[\frac{\Delta E_{n,p}}{kT} u + K_{n,p} u^{3/2}\right] du$$

$$K_{n,p} = \frac{4}{3} \frac{\sqrt{2m^\star \Delta E_{n,p}^3}}{e\hbar |F|} \tag{6}$$

The factors n_1 and p_1 depend on the difference between the trap-energy and the intrinsic energy and the intrinsic carrier density n_i. In the case of small electric fields, we obtain $\Gamma_{n,p} \ll 1$ and, thus, end up with the classical SRH-generation-recombination rate.

III. Results

Our simulations have been performed using the device simulator SENTAURUS. We studied a cylindrical nanowire TFET (see insert in Fig. 1) consisting of a 10^{20}cm^{-3} arsenic-doped drain region, opposite to a 10^{20}cm^{-3} boron-doped source region, and with a 10^{15}cm^{-3} boron-doped channel of 40 nm length and 30 nm diameter. The slope of the source/drain doping profiles is as steep as 2 nm/dec, and the gate stack is formed by a 2 nm SiO_2 layer and a TiN metallization. The resulting position-dependent energy band diagram calculated along a cutline parallel to the cylinder axis in a depth of 1 nm underneath the gate oxide for varying gate voltage (Fig. 1) demonstrates the formation of the tunneling region.

Fig. 2 displays the transfer characteristics of this nanowire TFET in n-operation mode. Here, n-operation mode stands for positive gate and drain voltages applied, while the source voltage is kept at zero volts as reference. Evidently this device exhibits a considerable on-current that is sustained by phonon-assisted tunneling. In addition we find a very good on-to-off current ratio with a very low blocking current. However, since the treshold voltage at the gate is shifted to higher values, when the drain voltage is increased, we observe an effect similar to the gate-induced drain leakage.

A. *Influence of quantum confinement*

Due to the fact that in MOS devices the electron density has its peak value not directly at the oxide-semiconductor interface, it is necessary to include the above-described quantum corrections in drift-diffusion-based device simulations in order to obtain realistic results. In the case of the investigated tunneling transistor the maximum of the quantum-corrected electron density is separated from the Si/SiO_2 interface in a distance of about 1 nm. Since the tunneling current is strongly dependent on the local charge densities the current flow through the channel region is quite sensitive to the effect of quantum confinement. This is clearly reflected in the transfer characteristics depicted in Fig. 3. Since quantum confinement reduces the electron density at the tunneling junction, the tunneling rate is lowered as well and, consequently, also the on-current.

B. *Variation of doping profiles*

We investigated the influence of variation of the doping profile on the device performance by analyzing cylindrical nanowire tunneling transistors which have the same size and channel doping as the structure discussed above, but different drain and source doping. It is shown that varying the peak doping concentration of the extensions does not affect the blocking current, while the on-current increases with rising doping concentrations. However, an undesired side-effect is that also the leakage current increases accordingly. This could be avoided by using high doping concentrations only on one side of the device. But unsymmetric doping profiles would make it necessary to design n- and p-type devices separately.

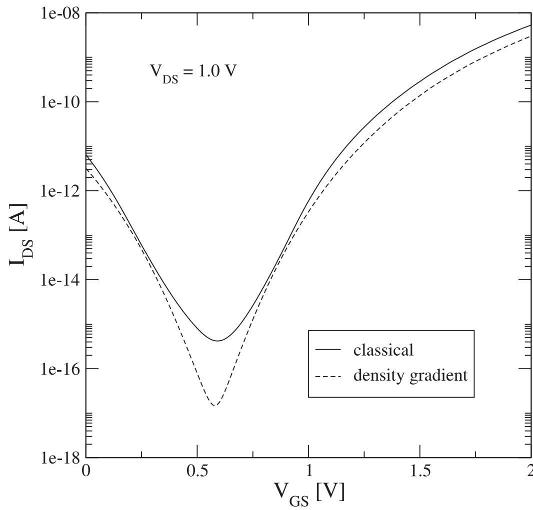

Fig. 3. Influence of quantum confinement under the gate oxid on the transfer characteristics of the nanowire TFET.

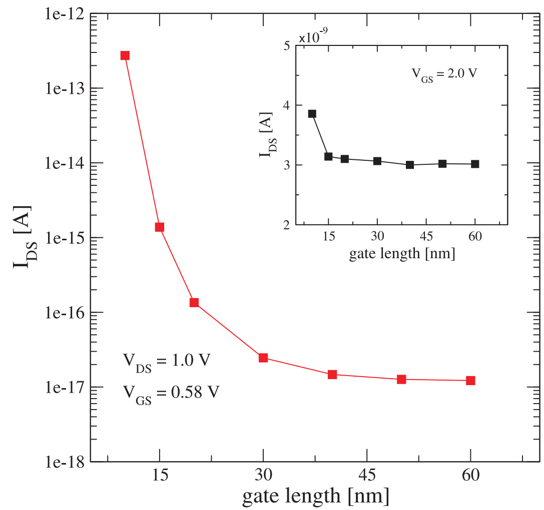

Fig. 5. On- and off-current of a nanowire TFET in dependence of the gate length (insert shows on-current).

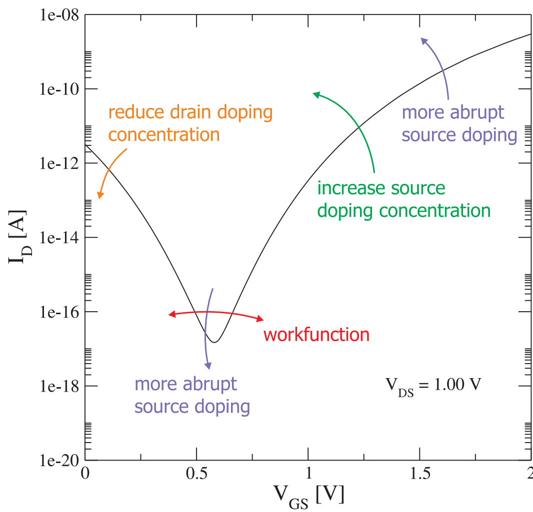

Fig. 4. Options for the optimization of the nanowire TFET by variation of the doping profile.

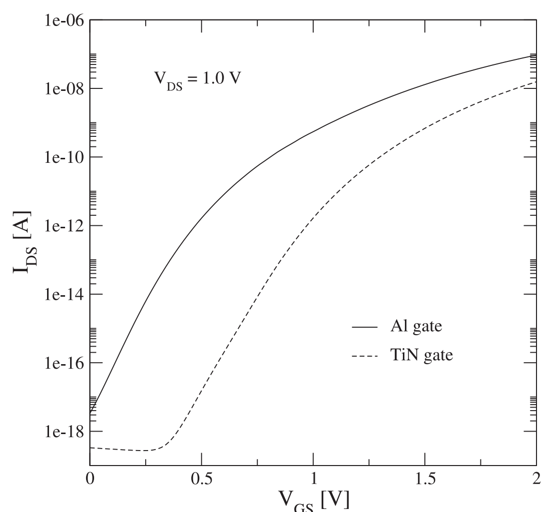

Fig. 6. Effect of different gate metallizations on the transfer characteristics of the nanowire TFET.

Another possible option for optimization is the use of more abrupt profiles, which leads to an increase of the on-current and a decrease of the blocking current at the same time and, therefore, also causes a steeper slope of the transfer characteristics. This is effected by the higher electric field and the more localized tunneling junction which reduces the off-current. An overview of the different possibilities for optimizing the device performance by the design of the doping profile is shown in Fig. 4.

C. Influence of scaling the device geometries

The scaling properties of nanometer MOS-devices are of fundamental interest. Hence we studied a wide range of geometrical modifications of nanowire TFETs and their effect on the scaling behavior. Since the gate length is a decisive factor for the space required by the device, we calculated the on- and off-currents of transistors with different gate length in n-operation mode (Fig. 5). The on-current is almost not affected, while the blocking current shows a significant rise for shorter gate lengths. But even in the case of 15 nm gate length we obtain a very good device characteristics. Considering that the doping gradient of source and drain is 2 nm/dec, the doping concentration in a channel region that is shorter than 15 nm cannot fall below a level of some 10^{17}cm^{-3}; hence we deal with a gated pn-junction rather than with a TFET. For n-type operation mode, this can be avoided by lowering the drain concentration so that the off-current is kept below an acceptable level. In this way it should be possible to build devices with less than 10 nm gate length which still exhibit reasonable transistor properties.

D. Material variations

A further optimization of the nanowire tunneling transistor could be expected from changing the configuration of the

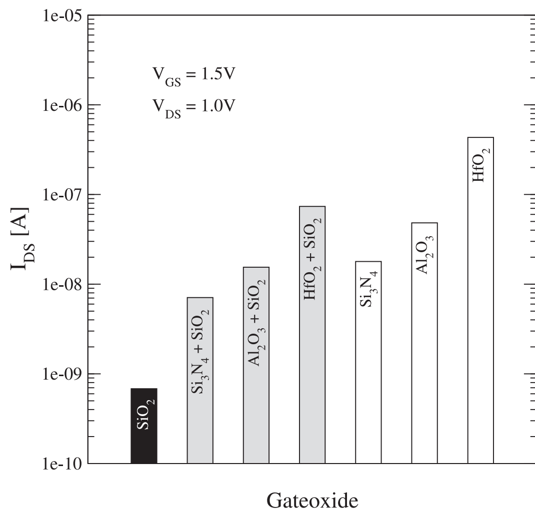

Fig. 7. Simulated on-currents (at $V_{DS} = 1.0V$ and $V_{GS} = 1.5V$) of the nanowire TFET for different gate-oxide material combinations.

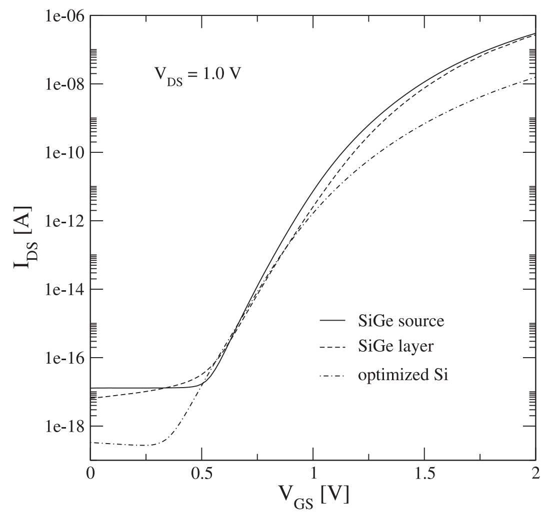

Fig. 9. Effect of SiGe source or delta-layer on the transfer characteristics of the nanowire TFET at $V_{DS} = 1.0V$.

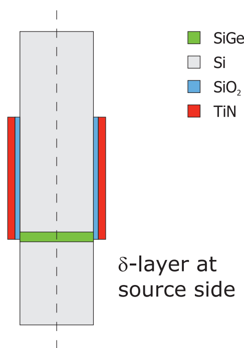

Fig. 8. Two alternative options of using SiGe in the source region of nanowire tunneling field-effect transistors.

gate stack. Changing the material of the gate metallization leads to a different workfunction which, in turn, shifts the treshold voltage (workfunction engineering). Fig. 6 illustrates the resulting effect on the transfer characteristics, when TiN is substituted for Al as gate material. Evidently Al is superior as gate material in the n-type operation mode.

An enhancement of the on-current of the nanowire tunneling transistor can be achieved by reducing the thickness of the gate oxide. The resulting higher electric field effects an increase of the tunneling rate and, thus, of the current. Alternatively, using high-k materials will show the same effect, but without the necessity of very thin gate oxides through which direct leakage tunneling occurs as parasitic effect. As shown in Fig. 7, the on-current becomes larger by three orders of magnitude, if HfO_2 is used as gate oxide material instead of SiO_2. Even the combination of $0.4\,\mathrm{nm}$ SiO_2 and $1.6\,\mathrm{nm}$ HfO_2 will raise the on-current by more than two orders of magnitude.

The integration of SiGe in the source region of the device results in a further improvement of the performance. Fig. 8 shows two alternative approaches: Placing a SiGe delta-layer directly at the heavily doped pn-junction, or building up the whole source region with SiGe. The effect on the transfer characteristics is displayed in Fig. 9: In both cases the on-current rises considerably compared to the Si reference structure, but at the same time also the off-current. Since the off-current is very small this increase by using SiGe is still tolerable.

IV. Conclusion

Using physics-based device simulation, which includes the quantum confinement of the charge carriers in the channel region and reproduce the tunneling processes, we performed a detailed numerical study of the behavior of a novel device that combines the concepts of the tunneling field-effect transistor and the multigate FET. The impact of variations of the most relevant design parameters (especially doping and geometry) on the device characteristics was evaluated with a view to the optimization of the device performance. Our finding is that downsizing nanowire tunneling transistors will not give rise to a loss in performance. We also investigated the possibilities to improve the devices by using high-k materials as gate oxide and SiGe in the source region and found that both approaches seem to be very promising.

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