

Effects of Quantum Confinement on Interface Trap Occupation in 4H-SiC MOSFETs

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Abstract— SiC MOSFETs suffer from an excessively high density of interface traps. Here, we present physical models to quantify the effect of quantum confinement in the channel of 4H-SiC MOSFETs on the occupation of interface traps. Quantum confinement in the MOSFET channel is solved for using the Density Gradient approach. Models for estimating the Fermi level at the interface, and thereby evaluating the occupation probability of interface traps are presented in the quantum confined scenario, and the results are compared to classical models. Significant difference is observed in trap occupation, especially at large gate biases, between the classical and quantum cases. This argues for the need for accurate modeling of confinement effects on interface trap occupation in 4H-SiC MOSFETs.

Keywords- Silicon Carbide MOSFET; density gradient; interface traps; quantum confinement

I. INTRODUCTION

Silicon Carbide (SiC) has a wide bandgap, high breakdown field, good thermal conductivity, and a native oxide, making it very attractive for design of high power high temperature electronics. However, excessively large densities of interface traps distributed over the 4H-SiC bandgap pose a serious concern for reliable and reproducible designs of SiC MOS devices [1, 2]. Therefore, accurate evaluation of the density, location and energy-distribution of these interface traps is very important for designing complex circuits using SiC devices. The distribution of mobile carriers in the channel becomes very important while calculating occupied interface trap densities. In this paper we investigate the occupation of traps while considering quantum confinement near the SiC-SiO₂ interface, and compare the results to a classical solution.

II. INTERFACE TRAP OCCUPATION

The occupied acceptor type interface trap density (N_{it}) depends on trap density of states (D_{it}) and the Fermi level at the interface. A typical trap density of states profile for 4H-SiC MOSFET is shown in Fig. 1. The values for D_{it} shown in the figure were extracted by comparing classical I_D - V_{GS} simulations to experiment [3].

Classical solution of transport in the SiC MOSFET gives the maximum of the electron concentration at the interface, leading to a large trap occupation. But, if quantum confinement is considered in the channel, then the peak of the electron

concentration is away from the interface, which may affect the occupation of the interface traps. This may then change the transport characteristics in SiC MOSFETs.

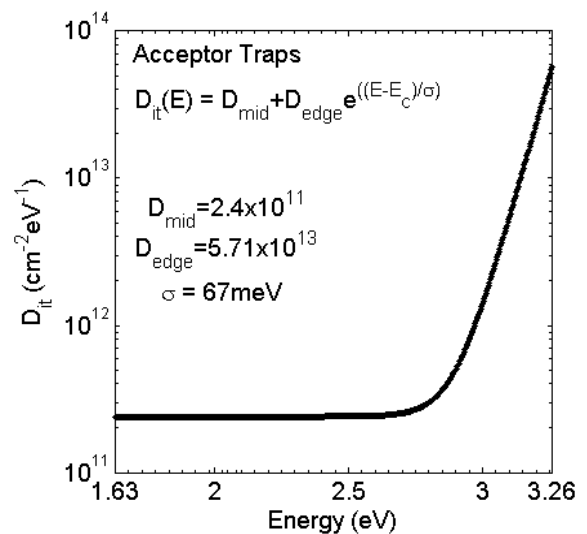


Fig. 1. Extracted interface trap density of states for the test 4H-SiC MOSFET by comparing simulated I_D - V_{GS} curves to experiment.

The occupied trap density at any position x along the interface, is given as in equation (1). Here, E_n and E_C are the neutrality point and the conduction band minima respectively, and $f(x, E)$ gives the trap occupation probability as a function of energy and position along the interface as defined by Fermi-Dirac statistics.

$$N_{it}(x) = \int_{E_n}^{E_C} D_{it}(E) f(x, E) dE \quad (1)$$

The trap occupation probability is calculated for the classical and the quantum cases by evaluating the location of the Fermi level (E_F) at the interface. For doubly degenerate trap occupation, the trap occupation probability is given as

$$f(x, E) = \frac{1}{1 + \frac{1}{2} \exp\left(\frac{E - E_F(x)}{k_B T}\right)} \quad (2)$$

Thus, evaluating the trap occupation involves correctly evaluating the location of the Fermi level at the interface. Calculating the Fermi level through classical and quantum approaches gives different trap occupations.

III. QUANTUM DEVICE SIMULATOR

Our custom 4H-SiC MOSFET 2-D Drift-Diffusion device simulator self-consistently solves the coupled Poisson, electron current continuity and hole current continuity equations everywhere in the device. To account for quantum effects, we incorporate the density gradient method, which gives rise to an effective quantum potential $\Delta\phi$. This potential is given by [4, 5]

$$\Delta\phi_{QM} = -\frac{\hbar^2}{2qm_y} \frac{1}{\sqrt{n}} \frac{\partial^2 \sqrt{n}}{\partial y^2} \quad (3)$$

Here, m_y and n are the electron effective mass and the electron concentration respectively, and \hbar is the reduced Planck's constant. We denote x and y as the directions parallel and perpendicular to the interface, respectively. We first solve the classical Drift-Diffusion system self-consistently. Then the quantum correction is calculated and the whole system is solved again to include the effects of quantum confinement.

IV. TRAP OCCUPATION PROBABILITY

The occupation of interface traps is calculated for the classical case and for the quantum confined case using different models. This requires the evaluation of the occupation probability function of equation (2), which then requires the knowledge of the Fermi level at the surface.

A. Classical Case:

The Fermi level at each point along the interface is calculated by using the classical electron concentration at the surface ($n(x,0)$) and the effective density of states at the conduction band minima (N_C) for 4H-SiC as

$$E_F(x) = E_C - \frac{k_B T}{q} \ln\left(\frac{n(x,0)}{N_C}\right) \quad (4)$$

B. QM Model I:

We follow the classical model methodology, but use the quantum surface electron concentration to calculate the Fermi level and thereby determine the trap occupation. This model does not provide details of the quantization of the conduction band. Due to quantum confinement, the conduction band will be split into quantized levels, thereby moving the conduction band minima to a level higher than E_C . This effect on energy quantization is included in the second quantum trap occupation model.

C. QM Model II:

Taking into account the splitting of the 3D conduction band into 2D sub-bands, the total inversion electron charge density (2-D electron density) for single sub-band occupation is written as [6, 7]

$$n_{inv}(x) = \frac{M_C m^* k_B T}{\pi \hbar^2} \ln\left[1 + \exp\left(\frac{E_F(x) - E_1(x)}{k_B T}\right)\right] \quad (5)$$

Where, n_{inv} is the 2-D electron inversion charge density, M_C is the valley degeneracy, m^* is the density of states effective mass, k_B is Boltzmann's constant, T is temperature, and E_1 is the first sub-band energy level.

By considering triangular quantum well approximation, the solution of the Schrodinger equation can be given in terms of Airy functions, and the first sub-band minimum can be written in terms of the effective surface electric field (F_S) as [6, 7, 8]

$$E_1(x) = E_C + \left(\frac{\hbar^2}{2m_y}\right)^{1/3} \left[\frac{9}{8} \pi q F_S(x)\right]^{2/3} \quad (6)$$

Here, E_C is the classical conduction band minima, and E_1 is the first sub-band energy level. The sub-band level is a function of position along the channel because the surface field varies from the source to the drain.

Using equations (5) and (6), and calculating the inversion layer charge density ($n_{inv}(x)$) from the self-consistent solution of electron concentration obtained through our device simulation, we can calculate the Fermi level that incorporates the effect of quantum confinement.

From the calculated Fermi levels, we evaluate the trap occupation in the classical and the two quantum model scenarios, to characterize the effect of confinement on device performance. The simulated device is a $424\mu\text{m} \times 5\mu\text{m}$ 4H-SiC MOSFET with a 48nm thick oxide. The threshold voltage at room temperature is approximately 3V.

V. RESULTS

We simulated the performance of the test 4H-SiC MOSFET using the classical and the two quantum models for calculating the interface trap occupation. We compared the classically simulated I_D - V_{GS} curves to experiment in order to extract the interface trap density of states of Fig. 1. Here we show some results of the trap occupation as a function of gate bias we obtained using the different models.

Fig. 2 shows the electron concentration as a function of depth away from the interface for the classical and quantum corrected cases at a gate-source voltage of 30V. As expected, quantum confinement at large gate bias caused a significant reduction in the electron concentration close to the interface.

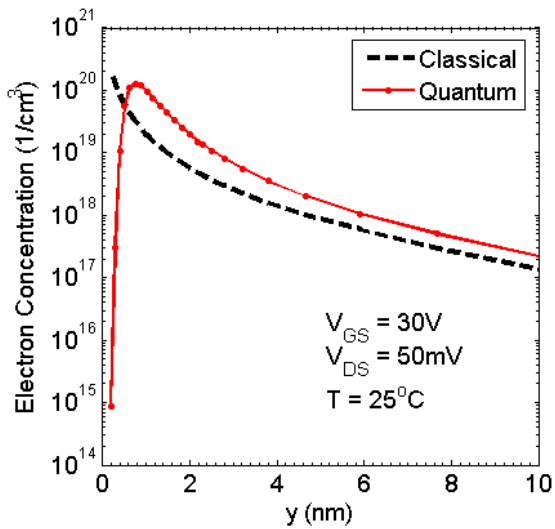


Fig. 2. Electron concentration as a function of distance away from the interface. The curve is plotted at the center of the channel.

Fig. 3 shows the occupied trap densities for the Classical and the QM Model I. Here, the Fermi level is calculated using the surface electron concentration alone. As the surface electron concentration drops due to quantum effects, for gate-source voltages between 0 and 15V, the occupied trap density predicted by QM Model I, is lower than the classical results. For V_{GS} between 15 and 30V, QM Model I predicts that the occupied trap densities are reduced even more. At higher temperatures, the channel confinement reduces and so the occupied trap densities in the quantum confined case calculated using the surface electron concentration alone, approach the classical values.

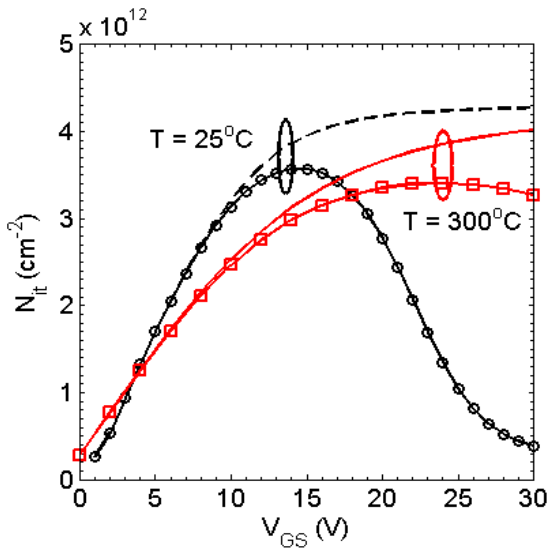


Fig. 3. Reduction of trap occupation due to quantum confinement as calculated by QM Model I. (Classical: Lines, QM Model I: Symbols). At high temperatures, trap occupation in the quantum case approaches the classical values.

The results for lower gate biases seem to make physical sense, in that the quantization tends to move the electrons away from the surface, and so it seems reasonable to expect that quantum confinement gives reduced values of occupied traps. However, as V_{GS} increases above 15V, it also seems reasonable that QM Model I over predicts the reduction in trap occupation. This is likely to be attributable to the fact the QM Model I uses only the surface electron concentration to calculate the Fermi level and ignores the probability of electrons further away from the interface becoming trapped.

Figure 4 shows the trap occupation calculated using the methodology outlined in QM Model II. This approach is more detailed than the previous one, because here we calculate the Fermi level relative to the first sub-band of the quantized conduction band. Furthermore, QM Model II removes the limitations intrinsic to QM Model I, because it allows for electrons in the entire inversion layer to contribute to trap occupation. It seems that physical intuitions would indicate that QM Model II may be over-predicting the population of occupied traps, because it assumes that electrons deeper into the channel also have a relatively high probability of occupying interface traps. As can be seen from the figure, the calculated trap occupation is slightly higher than the classical case.

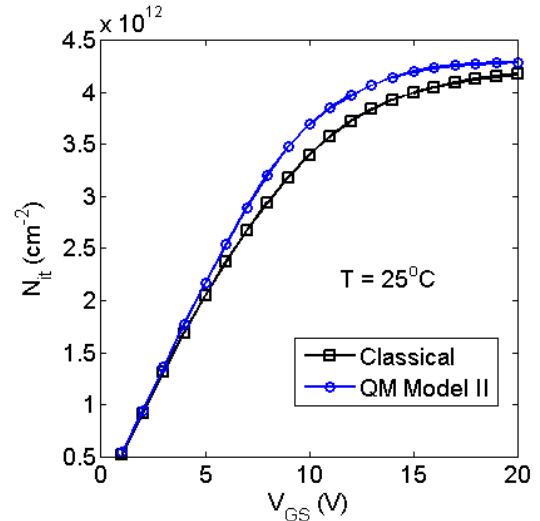


Fig. 4. Calculated occupied trap density using QM Model II and compared with the classical case. Slightly higher trap occupation seen in the quantum case at large gate biases.

Finally, in Fig. 5, we show the simulated I_D - V_{GS} characteristics for the Classical, QM Model I and QM Model II cases. The classical simulation has been fit to the experimental data and used to extract the density of states of Fig. 1.

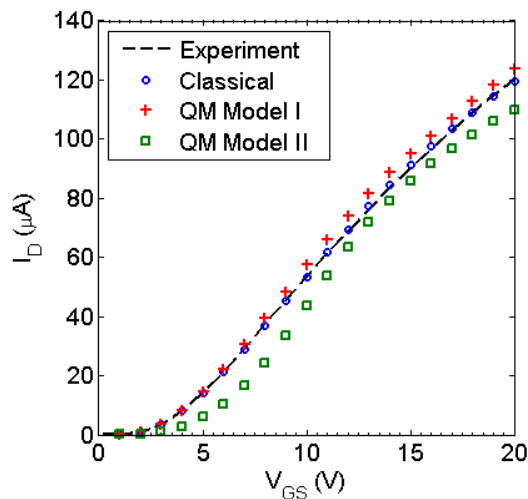


Fig. 5. Comparison of simulated room temperature classical and quantum corrected currents in the test 4H-SiC MOSFET to experiment.

We can clearly see that the I_D - V_{GS} curves obtained for the two quantum models differ from the classical case. Using any one of them to extract the interface trap density of states will give a slightly different value for the band-edge density of states, than the one extracted in the classical case. Therefore, it is important to use the most appropriate model for calculating the occupation probability while extracting the interface trap density of states for 4H-SiC MOSFETs. The extracted values for the mid-gap density will be unchanged as all three models approach the same trap occupation in the sub-threshold and near-threshold regions of operation.

VI. CONCLUSION

We employed the Density Gradient formalism to obtain an approximate solution of the Schrodinger equation near the interface in a 4H-SiC MOSFET to evaluate the effects of quantum confinement on interface trap occupation. We

compare two models for calculating the trap occupation when quantum confinement is considered. In the simple model (QM Model I) which uses only the surface electron concentration, the results show trap occupation reaching a maximum and then reducing with further increase in gate bias. A more detailed model (QM Model II), which includes the entire inversion layer and the quantization of the conduction band to calculate the Fermi level, shows trap occupation that is slightly above the classical case. We therefore conclude that even though current 4H-SiC MOSFETs are fabricated with thick oxides (>40nm), it would be worthwhile to consider quantum confinement while evaluating interface trap occupation.

REFERENCES

- [1] G. Pensl, M. Basler, F. Ciobanu, V. Afanasev, H. Yano, T. Kimoto and H. Matsunami, "Traps at the SiC/SiO₂ Interface," *Mat. Res. Soc. Symp.*, vol. 640, pp. H3.2.1-H3.2.11
- [2] H. Yano, T. Kimoto, and H. Matsunami, "Shallow states at SiO₂/4H-SiC interface on (1120) and (0001) faces," *Appl. Phys. Lett.*, vol. 81, pp. 301-303 (2002)
- [3] S. Potbhare, N. Goldsman, G. Pennington, A. Leles, and J. M. McGarrity, "Numerical and experimental characterization of 4H-silicon carbide lateral metal-oxide-semiconductor field-effect transistor," *J. Appl. Phys.*, vol. 100, 044515 (2006)
- [4] A. Akturk, G. Pennington and N. Goldsman, "Quantum Modeling and Proposed Designs of CNT-Embedded Nanoscale MOSFETs," *IEEE Trans. Elec. Dev.*, vol. 52, no. 4, pp.577-584 (2005)
- [5] M. G. Ancona and G. J. Iafrate, "Quantum Correction to the equation of state of an electron gas in a semiconductor," *Phys. Rev. B*, vol. 39, pp. 9536-40 (1989)
- [6] F. Stern and W. E. Howard, "Properties of Semiconductor Surface Inversion Layers in the Electric Quantum Limit," *Physical Review*, vol. 163, pp. 816-835 (1967)
- [7] H Wu, Y. Zhao, and M. H. White, "Quantum mechanical modeling of MOSFET gate leakage for high- k gate dielectrics," *Solid State Electronics*, vol. 50, pp. 1164-1169 (2006)
- [8] G. Pennington, "Electron transport simulations and band structure calculations of new materials for electronics: Silicon carbide and carbon nanotubes," Ph.D. dissertation, Univ. Maryland, College Park, MD, (2003)