3D Monte Carlo Simulation of Tri-Gate MOSFETs Using Tetrahedral Finite Elements

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***Abstract*—A parallel 3D Monte Carlo (MC) simulator designed to work on unstructured tetrahedral elements has been developed for the simulations of nano-MOSFETs. The 3D MC code is tested by the simulating a 10 nm gate length double gate (DG) MOSFET with a body thickness of 6.1 nm. We investigate in this device architecture the magnitude of the self-force arising because of the use of tetrahedral elements for the device mesh. Finally, the quantum corrections using density gradient approach are described and applied to a simulation of a 40 nm gate length TriGate MOSFET with a HfO_2 gate stack.**

I. Introduction

Various novel thin-body architectures have been proposed to tackle the degradation in performance observed in the conventional, bulk 32 nm technology and beyond. The thin-body transistors may be able to satisfy the requirements imposed by ITRS and continue the scaling. Accurate physical modelling of the carrier transport as well as a correct description of complex 3D geometry of these architectures is needed in order to predict their behaviour and optimise their design. Such physical modelling in nanoscale devices can be achieved via the ensemble Monte Carlo (MC) method. However, this technique is computationally very expensive for the complex 3D geometries as shown in the example of Fig. 1 [1], [2]. Therefore, the use of an optimal 3D mesh and parallel computing in order to save simulation time is imperative [3], [4] because the Poisson equation has to be solved on the device mesh at every in self-consistent simulations. Each iteration time step in self-consistent simulations depends on the geometry and doping of the device and it can be as small as 0.05 fs [5], leading to tens of thousands of iterations per bias point. Consequently, the need for a frequent solution of Poisson equation is the main bottleneck. Therefore, there is a need for MC device simulator which uses an optimal mesh and can discretise the simulation domains using non-rectangular meshes [6].

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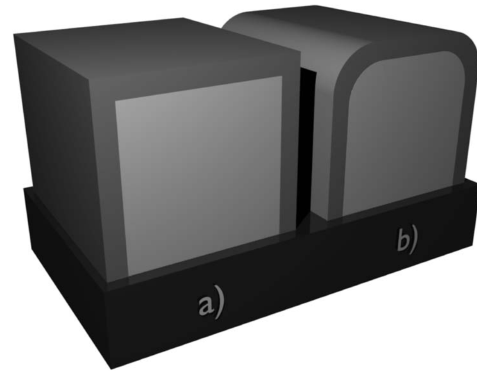

Fig. 1. Artistic view of TriGate MOSFET architecture with a) square corners and b) rounded corners.

In this work, we report on the development of a parallel 3D finite element simulator based on tetrahedral elements [7] and combined with an ensemble MC for bulk Si (Fig. 2). The parallelisation of the finite element solver is based on a domain decomposition strategy which has proved to be very efficient [8] (see Fig. 3), whereas a random distribution of particles among processors is used to parallelise the MC module. Firstly, we test the simulator on a double gate (DG) MOSFET architecture investigating the magnitude of the self-forces. After this test, we describe the simulation of a 40 nm gate length TriGate MOSFET, focusing on the implementation of the quantum corrections using the density gradient formalism [9].

II. Simulation Test: Double Gate MOSFET

The impact of the self-forces when we use tetrahedral elements is investigated by simulating a 10 nm gate length MOSFET with a body thickness of 6.1 nm and a source/drain doping of 1×10^{20} cm^{-3}. A distribution of the electric field on a particle alone in the device is illustrated in Fig. 4. We can see that the magnitude of electric field is relatively small near the centre. Furthermore, this electric field was close to zero if the boundaries were sufficiently far from the element enclosing the particle. This study also included the impact of different charge assignments on the I_D-V_G characteristics of

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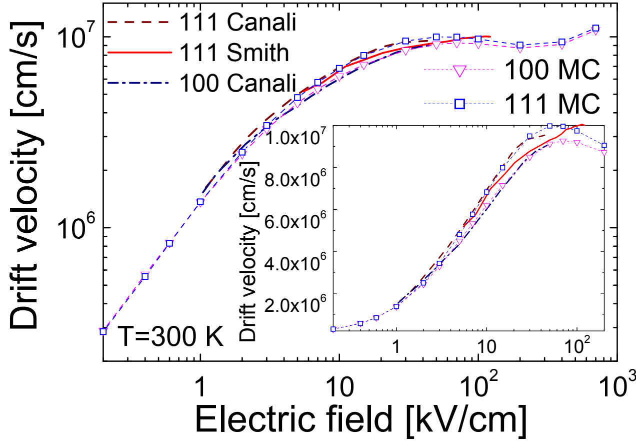

Fig. 2. Average electron velocity vs. applied electric field for bulk Si crystallographic indirections ⟨100⟩ and ⟨111⟩ compared with indicated experimental data. The inset shows the same data on a linear scale.

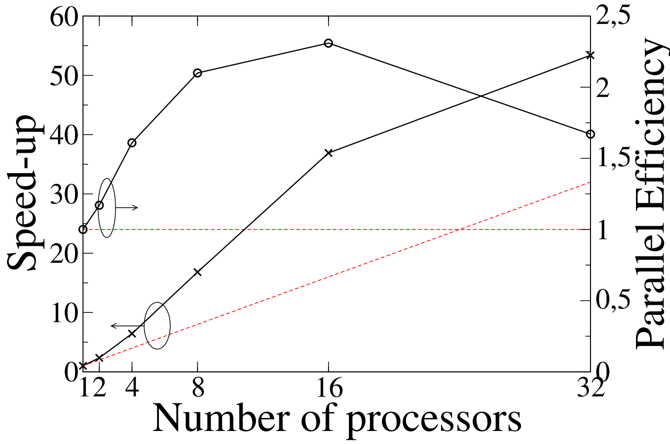

Fig. 3. Parallel efficiency (circles) and speed-up (crosses) of the 3D finite element MC simulator. The ideal values of linear scaling are also shown for comparison (dashed lines).

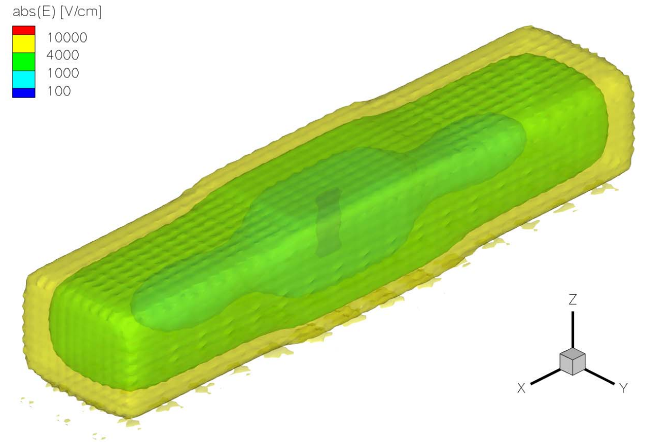

Fig. 4. Isosurfaces of the module of the electric field acting upon a particle positioned inside the device.

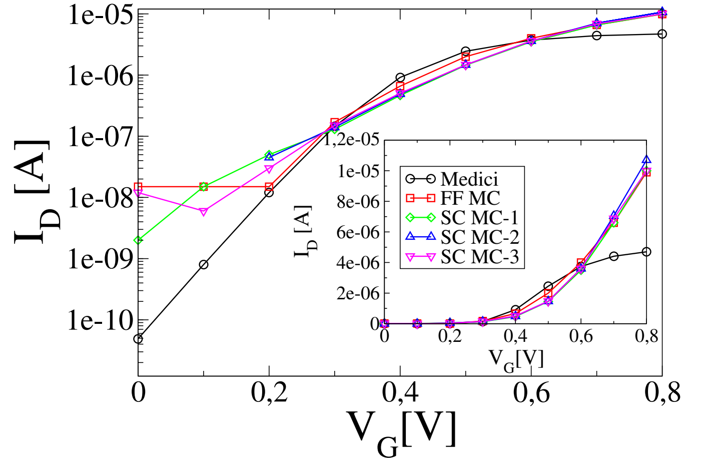

Fig. 5. I_D-V_G characteristics at V_D = 0.05 V of the 10 nm gate length, 6.1 nm thick body DG MOSFET obtained from different simulation approaches: a drift-diffusion (Medici [11]), a non self-consistent MC simulation (FF MC) and self-consistent MC simulations with three charge assignment schemes (SC MC-1,2,3).

the device as shown in Fig. 5. The charge assignment scheme using an average of the neighbouring inverse volumes (SC MC-3) have been selected as minimising the self-force [10].

III. Simulation of a 40 nm Gate Length Tri-Gate MOSFET

After testing the simulator we perform simulations on a Tri-Gate MOSFET architecture, described details elsewhere [1], with a FIN height of 27 nm and width of 23 nm. We have introduced rounded top and bottom corners to avoid high peaks in the electric fields and double threshold voltage [12], [13]. The top and bottom corner radii are 4 and 2 nm, respectively. The gate dielectric stack is composed by a 2 nm thick HfO_2 layer. The channel doping of the device is 1.0×10^{17} cm^{-3}, whereas the source and drain doping levels are 1.0×10^{20} cm^{-3}. The mesh for this structure is shown in Fig. 6, partitioned in eight subdomains using METIS [14] to perform a parallel execution of the code.

The quantum corrections are introduced through a quantum potential V_Q obtained using the density gradient model [15] by solving the following equation:

$$2b_n \frac{\nabla^2 \exp(u)}{\exp(u)} = 2u - V + V_n, \quad (1)$$

where $b_n = \frac{\hbar^2}{12m^*q}$ and the new variable $u = \frac{1}{2}(V - V_n + V_Q)$ has been introduced. A finite element discretisation is then applied resulting in the following system of equations:

$$\int_{\partial\Omega} 2b_n \theta_i \nabla(u) \vec{n} dS - \int_{\Omega} 2b_n \big(\nabla(\theta_i) - \theta_i \nabla(u)\big) \nabla(u) d\Omega =$$

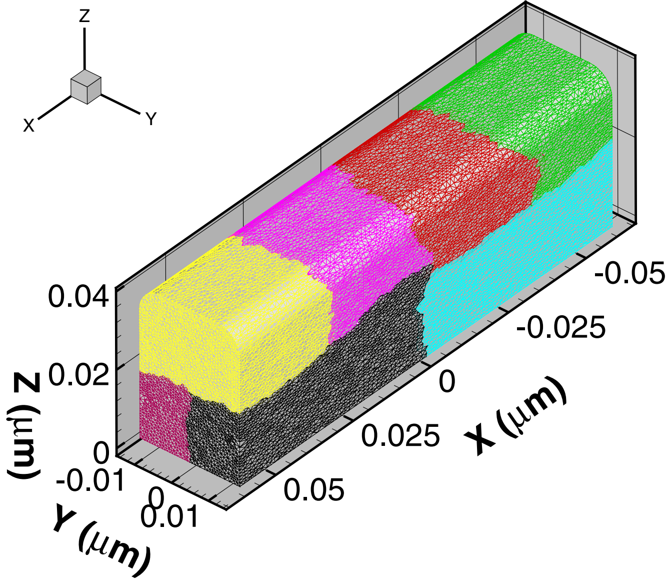

Fig. 6. Mesh of the simulated TriGate MOSFET with a FIN height of 27 nm, a width of 23 nm, a top corner radius of 4 nm and a gate dielectric stack composed by a 2 nm thick HfO_2 layer.

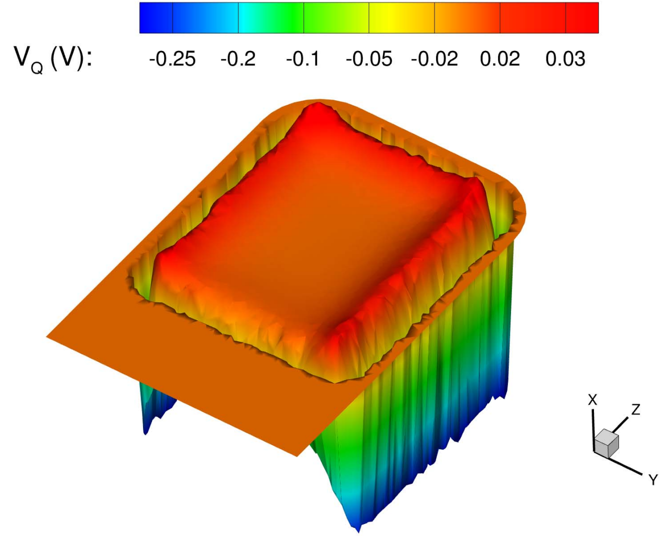

Fig. 7. Quantum potential in the cross-section of the device perpendicular to the source-drain direction in the middle of the gate ($x = 0$ plane).

$$\int_{\Omega}(2u - V + V_n)\theta_i d\Omega, \tag{2}$$

where θ_i are the finite element basis functions.

The use of the discretisation based on potentials instead of the standard based on carrier densities,

$$V_Q = 2b\frac{\nabla^2\sqrt{n}}{\sqrt{n}}, \tag{3}$$

allows a much smoother behaviour of electron density especially when it is used self-consistently [16], [17]. However, initially, we have only implemented it under a "frozen field" approximation, i.e., we calculate the correction only once from the solution of the drift-diffusion model used for the initialisation of the particles. Then, during the Monte Carlo simulation, we calculate the electric field used to move the carriers as

$$\mathbf{E} = -\nabla(V + V_Q^{FF}).$$

Figs. 7 and 8 show the quantum correction potential (V_D=0.05 V and V_G=1.1 V) in two cross sections of the device, the first one in the $x = 0$ plane and the second one in the $y = 0$ plane. Figures show that there will be a strong repulsion of the electrons from the interface coming from the quantum correction. It is interesting to note that this displacement of the peak charge density from the interface also brings numerical advantages, since collision detections with the interface are greatly diminished. This is especially important for the non-cartesian domains we are using, since in this case they require a high number of operations.

Fig. 9 shows the average electron concentration in a cross section of the device from the source end to the drain end after a simulation of 4 ps (V_D=0.05 V and V_G=1.1 V). We can see the repulsion from the Si/HfO_2 interface along the device. We also see the inversion in the three gated sides of the device, with a small penetration to the bottom, non-gated interface. Fig. 10 shows the average electron velocity in the x-direction along the device, from the source to the drain. We see that the peak mean velocity, near 1.9×10^6 cm·s^{-1}, is reached at the drain end of the channel.

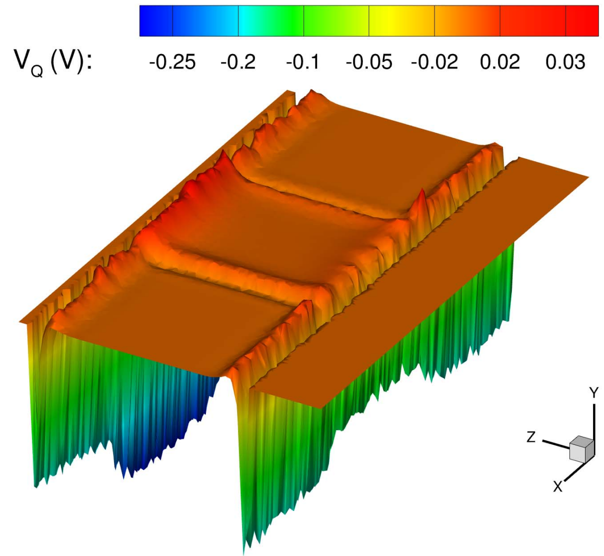

Fig. 8. Quantum potential in the cross-section of the device parallel to the source-drain direction in the middle of the device ($y = 0$ plane).

IV. Conclusion

We have described a parallel 3D device simulator based on the ensemble MC method to model the carrier transport and on the FE method to solve the Poisson equation on unstruc-

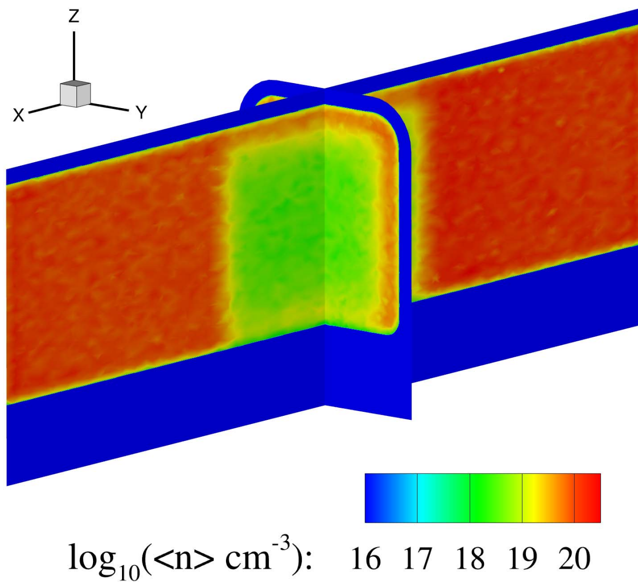

Fig. 9. Average electron concentration after 4 ps in the cross-sections of the device parallel and perpendicular to the source-drain direction in the middle of the device ($y = 0$ and $x = 0$ planes).

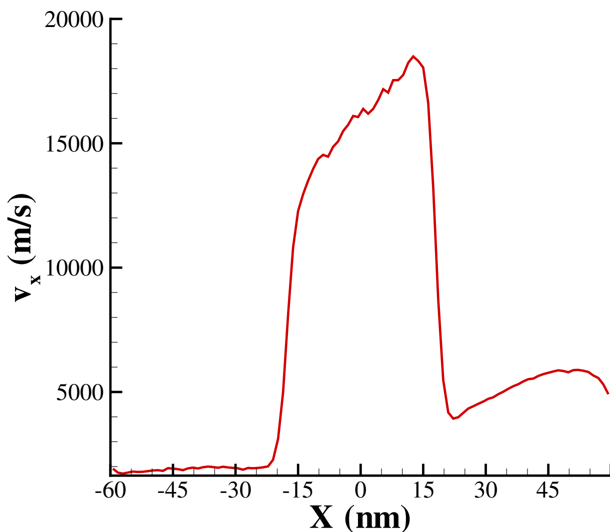

Fig. 10. Average electron velocity in the x-direction after a simulation of 4 ps with a time step of 0.1 ps along the device at V_D=0.05 V and V_G=1.1 V.

tured tetrahedral meshes. This device simulator is aimed for modelling of novel, thin-body transistor architectures with a complex 3D geometry. The code exhibits excellent parallel performance while keeping a maximum portability. First, we have presented a simulation example by modelling a 10 nm gate length Si DG MOSFET with a body thickness of 6.1 nm and a gate dielectric stack of 0.5 nm, showing a good agreement with the drift-diffusion simulations at a low gate voltage of 0.05 V. We have also shown the magnitude of the self-forces arising because of the use of tetrahedral elements. After this, we have presented the results from the simulations of a TriGate FinFET with rounded corners and a gate length of 40 nm. We have presented the approach how we have implemented the quantum corrections using density gradient method in the code. The quantum corrections due to carrier confinement will be a requirement when these architectures are scaled into even smaller gate lengths. We have presented preliminary results from the 3D MC device simulations at high gate and low drain voltages.

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