Ultra High Performance Insulator Channel Transistor

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***Abstract*—In this paper, an insulator channel planar transistor with ultra-high on-current, steep sub-threshold slope and superior scalability is presented. This device concept is proven by Sen Taurus device simulator with a quantum mechanic tunneling model and by a home made model utilizing transmission matrix theory.**

Keywords-insulator channel, on current, subthreshold slope, scalability

I. INTRODUCTION

With the continuous shrinking of the transistor dimensions, one of the big challenges for planar devices is to reach a low enough threshold voltage while keeping a low enough band-to-band leakage current [1-3]. There are some new planar structures [4-7] that utilize the tunneling effects in semiconductors and have ultra-low static power. However, these devices have very low drive current.

In this paper, a novel device concept is proposed, yielding both ultra high on current and ultra low off current. The channel composes of insulating material with discretionary selection of its work function and permittivity. The structural parameters are further optimized for achieving better performance.

II. DEVICE PHYSICS AND SIMULATION

The device structure is shown in Fig. 1, having a dielectric channel sandwiched by metal source and drain with a stack of gate insulator and electrode on top to provide vertical modulation. The mechanism of this device is essentially to control the tunneling current flow by modulating the barrier shape the carriers are facing. The initial barrier is configured to suppress the current. As the gate voltage ramps up, the profile of the potential energy is pressed downward, leading to a thinner tunneling barrier for the electrons and therefore higher drive current.

We use Sen Taurus [8] with non-local tunneling model [9] to simulate such devices. The model first calculates the tunneling probability under the arbitrary 2-D potential profile by using the local wave numbers and then transforms the tunneling probability into a virtual generation-recombination rate. Finally, it integrates the net generation rate over the entire device region to obtain aggregated current. On the other hand, we also develop a home made model to compare the results. This model evaluates the current by using the Tsu Esaki equation [10], in which the transmission probability for each energy level is plugged.

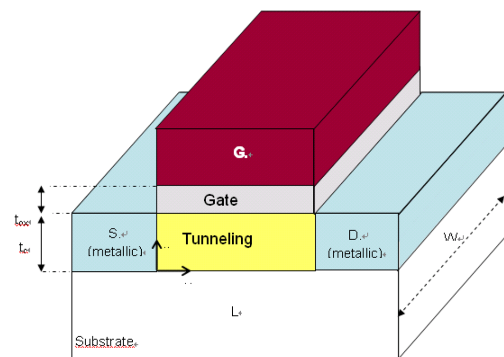

Fig.1: Illustration of the Insulator Channel Transistor.

The transmission probabilities are numerically solved by using transmission theory [11], the input of which is provided by numerically solving 2-D Poisson equation. The transfer characteristics of this device from both simulation methods are presented in Fig. 2. Both of the models give similar results. This is also true for devices with different structural and material parameters. As it is demonstrated in the figure, the ratio of on current to off current is higher than 1e5. The level of on current exceeds 1 mA/um while the off current is lower than 1nA/um. The potential profiles under different biases from simulation are shown in Fig. 3

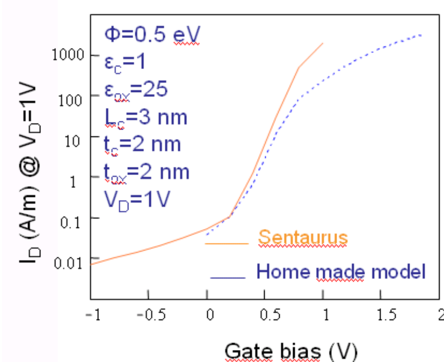

Fig.2: Comparison of the transfer characteristics between Sentaurus (solid line) and home made model (dash line) results.

Φ is barrier height, ε_c is permittivity for channel material, ε_{ox} is

permittivity for gate oxide, Lc is channel length, tc is body thickness, tox is gate oxide thickness, V_D is supply voltage.

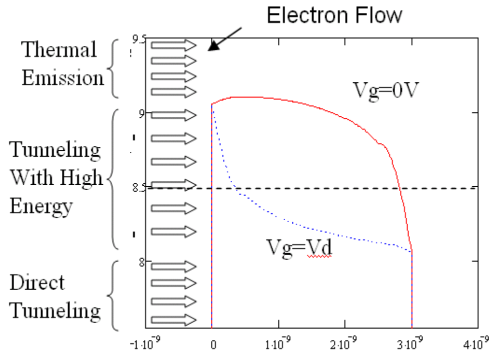

Fig.3: Potential energy along the channel with different gate biases simulated by home made model. Three components of the current are also illustrated.

The current composes of three components: thermal emission current whose energy is higher than the barrier, tunneling current with energy higher than the conduction band edge at the drain end and the direct tunneling current whose energy is lower than the conduction band edge at the drain end. The thermal emission current and the direct tunneling current are insensitive to the changing gate biases, and thus need to be avoided. With a channel length larger than 3nm, which is the channel range of our interest, the direct tunneling is negligible. For the thermal component, the following study is further done.

In our home made model, we decompose the current into tunneling and thermal emission part, as is plotted in Fig. 4. Clearly, the thermal emission dominates the sub-threshold region while the tunneling determines the magnitude of the drive current. Channel materials with high barrier will preclude the thermal emission but also yield low drive current while those with low barrier will lead to the opposite situation. Hence, the trade-off between the sub-threshold region and drive region needs to be considered when the material is chosen. Fig. 5 sketches I-V characteristics for different channel materials and Fig. 6 summarizes the trade-off with changing work function and power voltage.

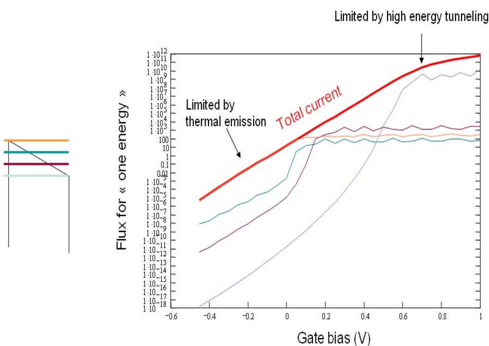

Fig.4: Transfer characteristics for current components with different energy levels.

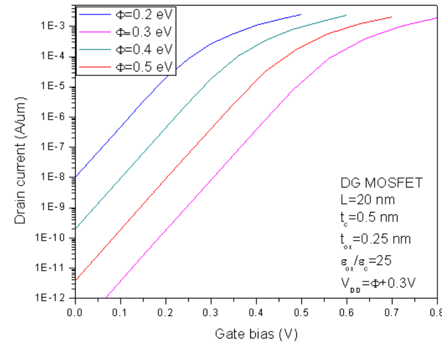

Fig.5: Transfer characteristics for channel materials with different work functions. Double-gate devices are used. The higher the work function is, the lower the current is.

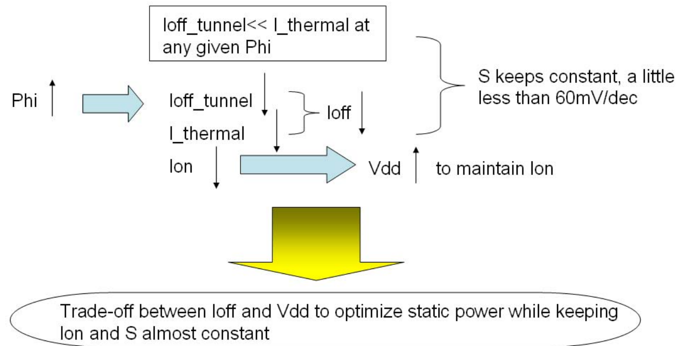

Fig.6: Illustration of trade-off between static power and speed when the work function is adjusted. Phi is the barrier height, Ioff_tunnel is the tunneling component, I_thermal is the thermal emission component, Ion is the total on current, Vdd is the power voltage and S is the subthreshold slope.

III. DEVICE OPTIMIZATION AND SCALABILITY

The fundamental rationale to improve the performance of this device is to suppress the direct tunneling and increase the sensitivity of the high-energy tunneling current to the changing potential shape. One of the most crucial factors is proven to be the channel thickness since the tunneling far away from the gate-channel interface tends to have less control and behave like direct tunneling. Devices with different body thickness are plotted in Fig. 7. As it is presented in the figure, the thicker the channel becomes, the worse the sub-threshold characteristic is due to the untamed direct tunneling. The device with a thickness of 2nm has impressive performance and is feasible for fabrication. Besides body thickness, the ratio of the permittivity between gate dielectric and channel dielectric is also influential to the controllability because higher ratio results in higher electric field in the channel according to electrostatics. As we show it in Fig. 8, the optimum case lies around a ratio of 5. Further increase of the ratio may only obtain marginal benefit. On the other hand, the device will still perform well with a ratio of 1, which provides us with flexibility on material selection.

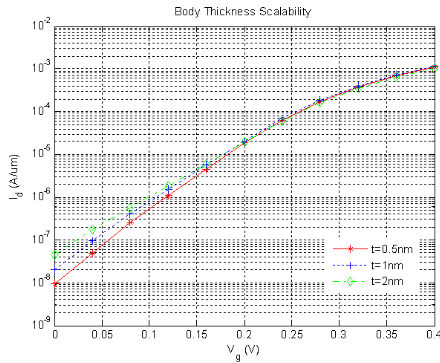

Fig.7: Transfer Characteristics for devices with different thicknesses.

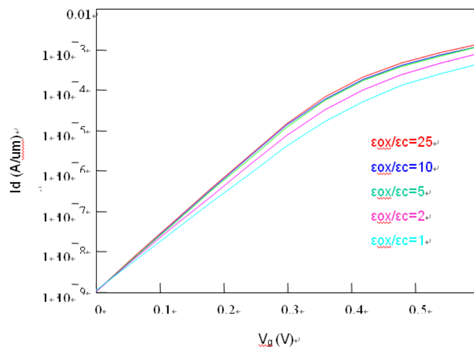

Fig .8: Transfer Characteristics with different permittivity ratios. The higher the ratio is, the higher the on current is.

From the simulation for the optimum case, off current reaches less than 1nA/um, on current achieves higher than 1mA/um, and source voltage stays as low as 0.35V. The sub-threshold slope maintains at around 60mV/dec. This case, however, is difficult to be implemented primarily because the dielectric that has both a high work function in order to obtain low barrier height normally has high permittivity. This indicates a low permittivity ratio between gate and channel and causes weaker gate control. Nonetheless, under such cases the device still yields impressive characteristics as is shown in Fig. 8.

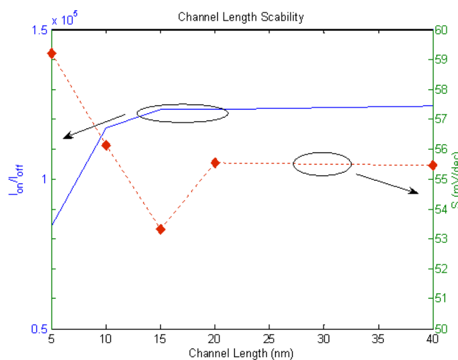

Fig.9: On and off current ratios and sub-threshold slope values for different channel lengths.

We now simulate a set of devices with different channel lengths to explore the scalability: 5nm, 10nm, 15nm, 20nm, and 40nm. As the channel length becomes shorter, the direct tunneling comes into play, which is not modulated by the gate bias and thus deteriorates the scalability. Nevertheless, as it is shown in Fig. 9, the device maintains its robustness even down to 5nm. The ratio between on and off current stays high above 5e4 and the sub-threshold slope keeps low at around 60. These results demonstrate that this novel structure has superior scalability although there does exist a physical limit.

IV. CONCLUSIONS

In this paper, we present a novel planar device structure that utilizes dielectric tunneling current as the drive current for transistors. From the simulations using Sen Taurus, a commercial device simulator, and a home made simulator, the results demonstrate the superior performance of the device. The on current stays above 1mA/um with a channel length of 5nm with ultra low power voltage of 0.35V. The off current is under 10nA/um with practical device dimensions.

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