Analytical Model for Point and Line Tunneling in a Tunnel Field-Effect Transistor

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***Abstract*—The tunnel field-effect transistor (TFET) is a promising candidate for the succession of the MOSFET at nanometer dimensions. In general, the TFET current can be decomposed into two components referred to as point tunneling and line tunneling. In this paper we derive a compact analytical model for the current due to point tunneling complementing the previously derived analytical model for line tunneling. We show that the derived analytical expression for point tunneling provides a more consistent estimate of the TFET current than a commercial device simulator. Both the line and point tunneling current do not show a fixed subthreshold-slope. Three key parameters for design of a TFET are: bandgap, dielectric thickness and source doping level. A small bandgap is beneficial for a high TFET on-current and a low onset voltage. Point tunneling and line tunneling show a strong dependance on gate dielectric thickness and doping concentration respectively.**

I. Introduction

As MOSFETs reach nanometer dimensions, exploration of alternative devices that possibly outperform the MOSFET at the nanometer scale is required. A promising alternative, which does not suffer from the fundamental subthreshold-slope limitation, is the tunnel field-effect transistor (TFET) in which the gate modulates the Band-to-Band Tunneling (BTBT) current between source and drain [1], [2]. Contrary to the MOSFET and the bipolar transistor, there is no simple analytical model available for the current of the general TFET configuration and this hampers a clear understanding of its working principle.

Wang discovered that the TFET current is composed of two components [3]. The first component "point tunneling" occurs at the source-channel interface and its dominant contribution is localized in a small area. The second component is located in the part of the source region overlapped by the gate. Because the area where BTBT starts from resembles a line, this component is called "line tunneling". An analytical model for line tunneling was recently derived yielding the total TFET current when the gate only covers the source area and point tunneling is negligible [4]. In the general case with the gate positioned over a part of the channel, point tunneling must also be considered.

In this paper we derive an analytical expression for the point tunneling current contribution (Section III) and briefly repeat the treatment for line tunneling (Section IV). In this way a compact expression is derived for the total TFET current.

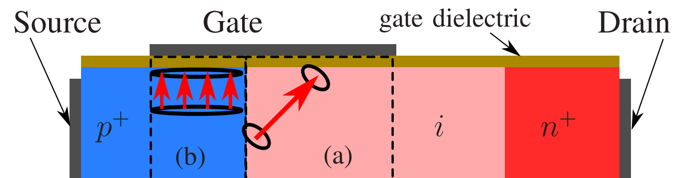

Fig. 1. General nTFET configuration with the region of point tunneling (a) and line tunneling (b) schematically indicated. The direction of BTBT in the semiconductor is indicated by arrows and the regions of highest tunneling efficiency are circumscribed by an ellipsoid. The support of the device (not shown) can either be bulk, insulator or a second gate as long as its influence on the electrostatic potential is negligible.

II. Current in a TFET

The TFET is generally described as a gated reverse biased p-i-n diode where the gate can be restricted to the area close to the source [5] as illustrated in Fig. 1. In our calculations line and point tunneling are treated separately and their contributions are added together to compute the total current.

For the calculation of the current we follow a strategy similar to that of a commercial device simulator [6]. First we determine the potential profile $\psi(\mathbf{r})$ in the area of interest. Next we determine the distance $l(\mathbf{r})$ an electron must travel to tunnel from valence to conduction band . Knowing the tunnel distance, the generation rate can be calculated using Kane's model as a function of the average electric field ($\mathcal{E} = E_g/l$) over the tunnel path:

$$G = A\frac{\mathcal{E}^{\mathcal{D}}}{\sqrt{E_G}}\exp\left(-BE_G{}^{3/2}/\mathcal{E}\right) \tag{1}$$

$$= A\frac{E_G^{D-1/2}}{q^D l^D}\exp\left(-Bq\sqrt{E_G}l\right) \tag{2}$$

with G the generation rate expressed in number of carriers per unit volume per unit time, E_G the bandgap, q the elementary charge and A, B and D material dependent parameters of Kane's model [7].

Finally the total TFET current is computed by integrating the generation rate and ignoring the p-i-n diode leakage current:

$$|I| = q\int G\mathrm{d}V \tag{3}$$

with $\mathrm{d}V$ an elementary volume in the device.

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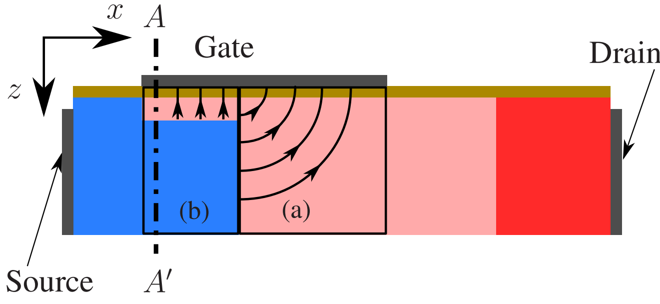

Fig. 2. Illustration of the electric field lines (black lines with arrows) in the channel (a) and under the gate in the depleted region (b) for the structure from Fig. 1. A two-dimensional potential profile is present in the intrinsic region and at high gate bias a significant depletion region will emerge under the gate.

The drain is typically located some distance away from the source and generally has little direct impact on the electrostatics of the tunnel barrier. As a consequence only the gate and source contact determine the potential in the following treatment, obscuring the influence of the drain voltage.

For low drain voltages the actual device current will be lower than our calculated results if the conduction band is occupied, this can be mediated by restricting the area of integration. For degenerately doped semiconductors, the device current will be lower because the valence band is not completely occupied. At high currents, the lower actual device current can be interpreted as the consequence of a resistance in series with the tunnel barrier. The main reason for an overestimation of the actual device current is the absence of a self-consistent determination of the potential in our calculations.

III. Point tunneling

In this section we consider the two-dimensional tunneling at the source-channel interface.

When a positive gate voltage is applied, a depletion region at the source-channel interface is formed, the channel potential profile changes and a limited amount of charge will flow into the channel from the drain. In the case of a highly doped source – which is beneficial to achieving a high on-current – a small depletion region is enough to provide a significant electric field in the channel.

To describe the potential, we adopt the x and z direction as shown in Fig. 2 and assign the coordinate $x = 0$ to the source-channel interface and the coordinate $z = 0$ to the gate-gate dielectric interface.

To determine the potential profile we make four assumptions. A first assumption is that the potential drop due to depletion in the source is negligible and the potential at $x = 0$ equals the source potential. Secondly, we assume the influence of the charge in the channel on the channel potential can be neglected. A third assumption is the absence of charge in the gate dielectric and a fourth assumption is that gate dielectrics with identical electrical thickness will result in an identical potential profile in the intrinsic region. For the remainder of our treatment, we use a semiconductor equivalent thickness:

$$t'_{\rm ox} = t_{\rm ox}\frac{\epsilon_{\rm s}}{\epsilon_{\rm ox}} \tag{4}$$

with $\epsilon_{\rm s}$ and $\epsilon_{\rm ox}$ the semiconductor and gate dielectric constant respectively and $t_{\rm ox}$ is the physical dielectric thickness.

The potential in the channel and in the gate dielectric satisfy Poisson's equation

$$\nabla^2\psi = -\frac{\rho}{\epsilon_{\rm s}} \tag{5}$$

with ψ the potential taken at the semiconductor valence band edge and ρ the charge density.

As a consequence of our second, third and fourth assumption, $\rho = 0$ in the intrinsic semiconductor and gate dielectric region and the equation reduces to Laplace's equation. Moreover, the electrostatic potential is to obey the boundary conditions:

$$\psi(0,z) = \psi_{\rm s} \quad , \quad \psi(x,0) = \psi_{\rm g} \tag{6}$$

where $\psi_{\rm g}$ and $\psi_{\rm s}$ are the potential in the source and gate respectively. For convenience, we take $\psi_{\rm s} = 0$, the gate potential is then related to the applied gate voltage $V_{\rm gs}$ by:

$$\psi_{\rm g} = V_{\rm gs} - V_{\rm FB} \tag{7}$$

with $V_{\rm FB}$ the flatband voltage.

Assuming the semiconductor extends towards infinity for ($x > 0$ and $z > 0$), the solution for the potential is most easily given in polar coordinates ($x = r\sin\theta$ and $z = r\cos\theta$):

$$\psi(x,z) = \psi_{\rm g}\frac{2}{\pi}\theta \quad ; \quad 0 \le \theta \le \frac{\pi}{2} \tag{8}$$

In the case of our two-dimensional potential, the tunnel path length is computed as the length of an arc along an electric field line:

$$l = r\theta_0 \tag{9}$$

with $\theta_0 = \pi E_{\rm G}/(2q\psi_{\rm g})$ the angle between two equipotential lines with a potential difference equal to $E_{\rm g}/q$.

We calculate the total current by integrating the generated charge over the entire area where tunneling occurs as shown in Fig. 3:

$$I = qW\int_{r_0}^{\infty}\int_{\theta_0}^{\arccos(t'_{\rm ox}/r)} G(r)r\,{\rm d}\theta\,{\rm d}r \tag{10}$$

$$= WA\int_{r_0}^{\infty}(\arccos(t'_{\rm ox}/r) - \theta_0)\frac{E_{\rm G}^{D-\frac{1}{2}}e^{-Bq\sqrt{E_{\rm G}}r\theta_0}}{q^{D-1}r^{D-1}\theta_0^D}{\rm d}r \tag{11}$$

with $r_0 = t'_{\rm ox}/\cos(\theta_0)$.

Making a first order Taylor expansion around $r = r_0$, we integrate by parts and neglecting $\cos(\theta_0)$ with respect to unity to get:

$$I \approx \frac{WAE_{\rm G}^{D-\frac{1}{2}}}{q^{D-1}r_0^{D-1}\theta_0{}^D}\int_{r_0}^{\infty}\frac{t'_{\rm ox}(r-r_0)e^{-Bq\sqrt{E_{\rm G}}r\theta_0}}{\sqrt{1-(t'_{\rm ox}/r_0)^2}r_0^2}{\rm d}r \tag{12}$$

$$\approx \frac{WAE_{\rm G}^{D-\frac{3}{2}}t'_{\rm ox}}{q^{D-1}B^2}\frac{1}{\theta_0^{D+2}r_0^{D+1}}e^{-Bq\sqrt{E_{\rm G}}r_0\theta_0} \tag{13}$$

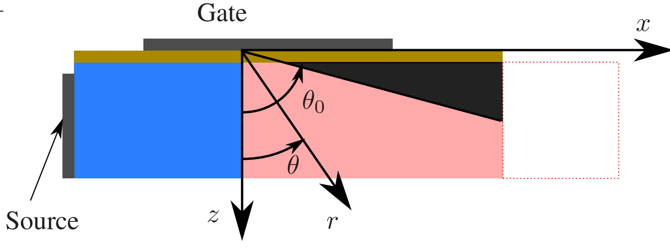

Fig. 3. Area over which the generation rate must be integrated for point tunneling (black) where the source-channel interface is shown on the left (blue-pink) and the gate-gate dielectric interface on top (grey-brown). The structure is assumed to extend towards infinity at the bottom and at the right.

To come to a polynomial pre-factor we approximate r_0 as a function of the gate potential

$$r_0 = t'_{\mathrm{ox}}/\sin\left(\frac{\pi(q\psi_{\mathrm{g}} - E_{\mathrm{G}})}{2q\psi_{\mathrm{g}}}\right) \approx t'_{\mathrm{ox}}\frac{2q\psi_{\mathrm{g}}}{\pi(q\psi_{\mathrm{g}} - E_{\mathrm{G}})} \quad (14)$$

Substituting Eq. (14), the value of θ_0 and the default value of $D = 2$ into Eq. (13):

$$I = WT\frac{q\psi_{\mathrm{g}}}{E_{\mathrm{G}}}\left(\frac{q\psi_{\mathrm{g}}}{E_{\mathrm{G}}} - 1\right)^3 e^{S/(q\psi_{\mathrm{g}}/E_{\mathrm{G}}-1)} \quad (15)$$

with ψ_{g} given by Eq. (7) and

$$T = \frac{2A\sqrt{E_{\mathrm{G}}}}{\pi q^3 B^2 {t'_{\mathrm{ox}}}^2} \quad , \quad S = -Bq\sqrt{E_{\mathrm{G}}}t'_{\mathrm{ox}} \quad (16)$$

A comparison between Eq. (15) and device simulation results for the structure of Fig. 1 and its pTFET equivalent is shown in Fig. 5 and Fig. 6 respectively. Around the onset of tunneling an asymmetry between the nTFET and the pTFET can be seen from the device simulations. This indicates that the device simulator overestimates the nTFET current and underestimates the pTFET current. Since our calculated results are consistent, they can be considered more accurate in this region of interest.

Eq. (15) reveals that the on-current due to point tunneling has a strong dependence on the bandgap and dielectric thickness. A smaller bandgap will lead to a smaller onset voltage $V_{\mathrm{onset}} = V_{\mathrm{FB}} + E_{\mathrm{g}}$. A high doping level is assumed in our approximations and will also be beneficial for a reduction of the onset voltage as a higher doping level will change the metal-semiconductor flatband voltage.

IV. Line Tunneling

In this section we consider tunneling in the source region in the direction normal to the gate, this contribution will be important at high gate voltages.

When applying a positive gate voltage, a depletion region will be formed and a one dimensional treatment of the potential can be performed. At higher gate voltages, an inversion layer can be formed but as the inversion layer electrons significantly occupy the conduction band, we may ignore their contribution to the BTBT generation current and evaluate the latter for the depletion region only. This treatment leads to an analytical formula for the line tunneling current [4] which is briefly repeated here.

The total line tunneling current I can be computed as the sum over all charge generated by BTBT per unit time:

$$I = \frac{qWLA}{2}\int_{l_1}^{l_2}\frac{E_{\mathrm{G}}^{D-\frac{1}{2}}}{q^D l^D}e^{-Bq\sqrt{E_{\mathrm{G}}}l}\left(1 - \frac{2E_{\mathrm{G}}\epsilon_{\mathrm{s}}}{q^2N_{\mathrm{a}}}\frac{1}{l^2}\right)\mathrm{d}l \quad (17)$$

where l denotes the tunnel path length ranging from l_1 to l_2 in the depletion region as shown in Fig. 4. L is the gate overlap length and N_a is the doping concentration.

Assuming that the exponential terms change much more rapidly than the polynomial terms under a variation of l and substituting D by its default value of 2, we obtain closed expressions for the current I and onset voltage V_{onset} as a function of the gate voltage V_{gs}:

$$I \approx WLTe^{S\sqrt{V_{\mathrm{gs}}-V_{\mathrm{onset}}}}\sqrt{V_{\mathrm{gs}} - V_{\mathrm{onset}}} \quad (18)$$

$$V_{\mathrm{onset}} = V_{\mathrm{FB}} + \frac{E_{\mathrm{G}}}{q}\left(1 + 2t_{\mathrm{ox}}\frac{\epsilon_{\mathrm{s}}}{\epsilon_{\mathrm{ox}}}\sqrt{\frac{q^2N_{\mathrm{a}}}{2E_{\mathrm{G}}\epsilon_{\mathrm{s}}}}\right) \quad (19)$$

with

$$T = q\frac{A}{Bq^{3/2}}\frac{qN_{\mathrm{a}}}{2\epsilon_{\mathrm{s}}}\sqrt{\frac{1}{E_{\mathrm{G}}\gamma}}e^{-BqE_{\mathrm{G}}\sqrt{2\epsilon_{\mathrm{s}}}/\sqrt{q^2N_{\mathrm{a}}}}, \quad (20)$$

$$S = Bq\sqrt{\frac{2E_{\mathrm{G}}\epsilon_{\mathrm{s}}}{qN_{\mathrm{a}}}\frac{1}{\gamma}}, \quad \gamma = 1 + t_{\mathrm{ox}}\frac{\epsilon_{\mathrm{s}}}{\epsilon_{\mathrm{ox}}}\sqrt{\frac{q^2N_{\mathrm{a}}}{2E_{\mathrm{G}}\epsilon_{\mathrm{s}}}} \quad (21)$$

To obtain Eq. (17), we made the assumption that the TFET current equals the generation current in the depletion region under the source. We validate this assumption by comparing the derived formulas with Medici simulation results in Fig. 7. The analytical results agree very well with the non-selfconsistent calculations by Medici. For large gate voltages, the channel resistance in series with the tunnel barrier is no longer negligible and the self-consistently calculated current saturates.

Eq. (19) provides the line tunneling current of the TFET as a function of gate voltage when the device parameters are known. Clearly, the square root dependence indicates the absence of a 60 mV/decade subthreshold-slope. The on-current increases with decreasing bandgap and higher doping level. A small bandgap also reduces the onset voltage and will be aimed at as far as it does not jeopardize the TFET off-current. An upper limit on the onset voltage or on the voltage drop over the dielectric will limit the doping level. Finally, enabling the gate to adequately control the source region, a small dielectric thickness will improve the validity of the approximations.

V. Conclusion

We have shown an approximating analytical description of the TFET potential profile in the channel and in the region under the gate. Using this potential profile and adopting Kane's Model, we derived an approximating compact formula for the point tunneling current complementing the analytical model for line tunneling. The approximations accompanying this derivation are justified by observing agreement with device

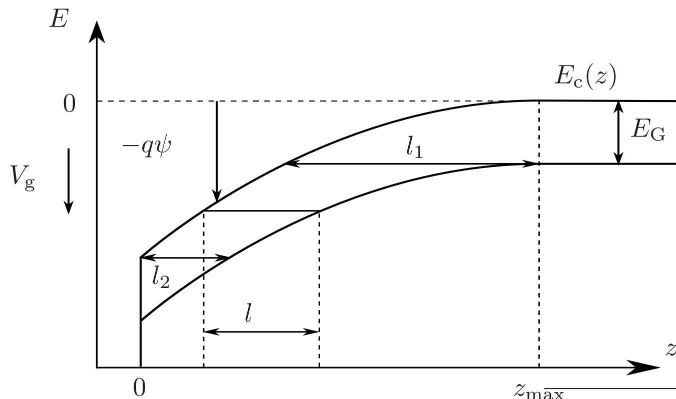

Fig. 4. Band diagram of the cross-section A-A' from Fig. 2 indicating the tunneling distance l for line tunneling. ψ is the electrostatic potential, E_c is the conduction band energy and V_g the gate voltage (as shown in [4]).

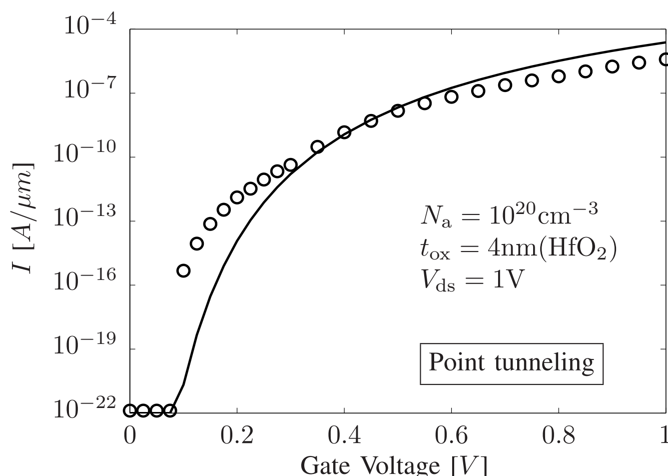

Fig. 5. Comparison between analytical model for point tunneling (solid line) and Medici calculations (○) for a silicon nTFET with a structure as shown in Fig. 1.

simulation results in the case of line tunneling. In the case of point tunneling, the current calculated by the device simulator Medici shows a discrepancy with our model due to an over- and underestimation in the case of the n- and pTFET respectively and our result can be considered more accurate.

The three key parameters for the TFET current derived from our formulas are: bandgap, dielectric thickness and source doping level. In both the case of point and line tunneling a lower bandgap will lead to an improved on-current and a lower onset voltage. A low bandgap will therefore be aimed at for a TFET as long as the deterioration of the off-current is acceptable. A reduced dielectric thickness will reduce the onset voltage of line tunneling and will significantly improve the current of point tunneling. An increased doping concentration reduces the point tunneling onset voltage while it increases the line tunneling onset voltage but at the same time the line tunneling on-current increases.

Acknowledgments: The authors would like to thank An De Keersgieter for support with the Medici simulations.

This work was supported by IMEC's Industrial Affiliation Program. Anne S. Verhulst acknowledges the support of a Marie Curie International Reintegration Grant within the 6th European Community Framework Programme, as well as a postdoctoral fellowship of the Fund for Scientific Research - Flanders.

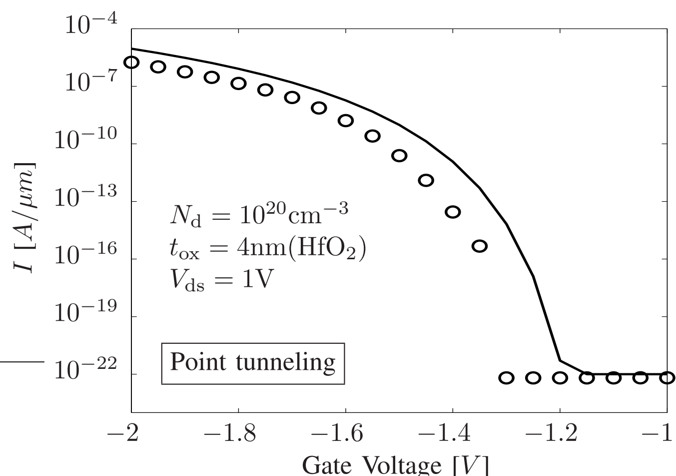

Fig. 6. Comparison between analytical model for point tunneling (solid line) and Medici calculations (○) for a silicon pTFET with a structure as shown in Fig. 1.

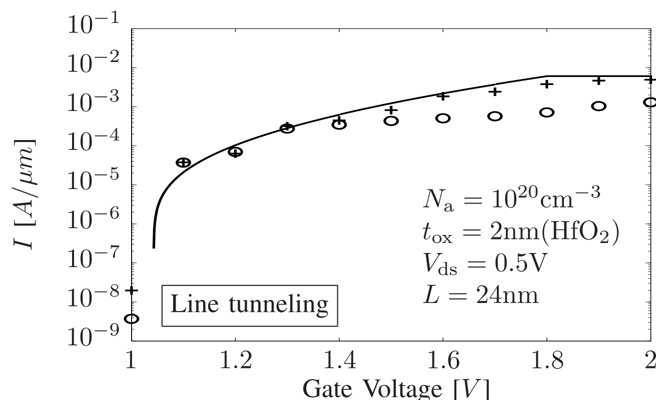

Fig. 7. Analytical formula (18) (solid) with the gate voltage limited to the inversion onset voltage compared with self-consistent device simulations (○) and non-selfconsistent device simulations (+) for a Si TFET with the gate only on top of the source compared with (as shown in [4]).

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