Is Dual Gate Device Structure Better From Thermal Perspective?

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***Abstract* — Heating effects are investigated in dual-gate devices using an in-house thermal particle-based device simulator. Our simulation results demonstrate that the dual-gate device structure is advantageous even though there is slightly higher current degradation due to lattice heating compared to conventional single gate structures, since the magnitude of the on-current is 1.5-1.8 times larger in this structure. Thus, one can trade off a slight increase in current degradation due to lattice heating for more current drive.**

Keywords - DG devices, particle-based simulations, heating effects, hot phonons

I. INTRODUCTION

One of the primary reasons for device degradation at shorter channel lengths in FD SOI devices is the encroachment of drain electric field in the channel region. As shown in Fig. 1, the gate electrode shields the channel region from those lines at the top of the device, but electric field lines penetrate the device laterally and from underneath, through the buried oxide and the silicon wafer substrate causing the undesirable DIBL for the charge carriers.

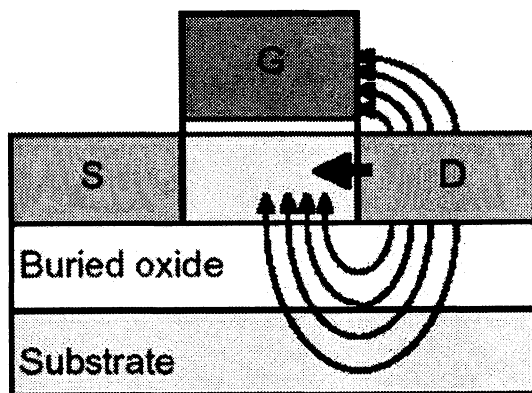

Fig. 1. Electric field lines from the drain.

To prevent the encroachment of electric field lines from the drain on the channel region, special gate structures can be used as shown in Fig. 2. Such "multiple-gate" devices include double-gate transistors, triple-gate devices such as the quantum wire [1], the FinFET [2] and Π-channel SOI MOSFET [3], and quadruple-gate devices such as the gate-all-around device [4], the DELTA transistor [5], and vertical pillar MOSFETs [6].

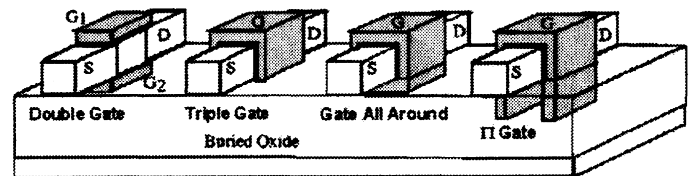

Fig. 2. Double-gate, triple-gate, gate all around (GAA), and Π-gate SOI MOSFETs.

The double-gate device structure allows for termination of the drain electric field at the gates and leads to a more scalable FET. The double-gate concept was first reported in 1984 [7] and has been fabricated by several groups since then. The salient features of the DG FET (Fig. 2) are: (1) control of short-channel effects by device geometry, as compared to bulk FET, where the short-channel effects are controlled by doping (channel doping and/or halo doping); and (2) a thin silicon channel leading to tight coupling of the gate potential with the channel potential. These features provide potential DG FET advantages that include: (1) reduced 2D short-channel effects leading to a shorter allowable channel length compared to bulk FET; (2) a sharper subthreshold slope (60 mV/dec compared to 80 mV/dec for bulk FET) which allows for a larger gate overdrive for the same power supply and the same off-current; and (3) better carrier transport as the channel doping is reduced (in principle, the channel can be undoped). Reduction of channel doping also relieves a key scaling limitation due to the drain-to-body band-to-band tunneling leakage current. A further potential advantage is more current drive (or gate capacitance) per device area; however, this density improvement depends critically on the specific fabrication methods employed and is not intrinsic to the device structure. The most common mode of operation of the DG FET is to switch the two gates simultaneously.

The purpose of this work is to examine the advantages of a double-gate structure from a thermal perspective. The paper is organized as follows: Brief description of the simulator is given in Section II, simulation results for the double-gate

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structure from Fig. 2 are presented in Section III and in section IV we present our conclusive comments regarding this work.

II. THEORETICAL MODEL

To investigate lattice heating within a Monte Carlo device simulation framework, we simultaneously solve the Boltzmann transport equation for the electrons [8], the 2D Poisson equation to get the self-consistent fields and the hydrodynamic equations for acoustic and optical phonons. The phonon temperature then determines the choice of the scattering table. The exchange of variables between the electron particle-based device simulation part and the self-consistently coupled energy balance solver is presented in Figure 3 [9,10].

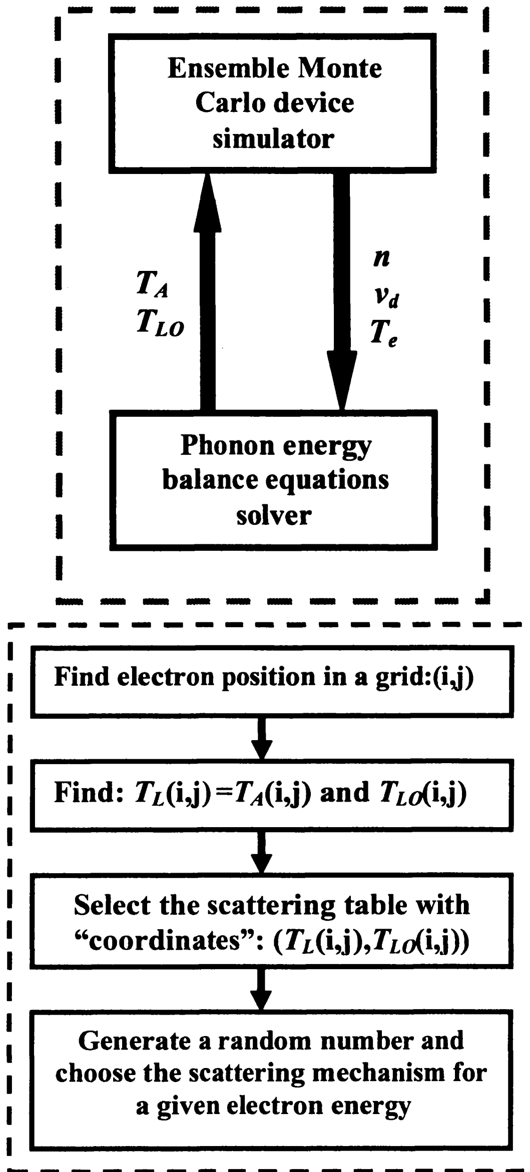


Fig. 3. Top panel – Exchange of variables between the two transport kernels. Here T_A is the acoustic/lattice temperature, T_{LO} is the longitudinal optical phonons temperatures, n is the electron density, v_d is the drift velocity and T_e is the electron temperature. Bottom panel: Choice of the proper scattering table. (i,j) are node points within a two-dimensional mesh.

The bottom of the buried oxide layer (BOX) is assumed to be isothermal boundary and the temperature at that boundary is set to 300K. Another isothermal contact is the gate and the gate temperature is varied between 300 - 600 K. It is important to note that it takes only 4 - 5 Gummel cycles to get convergence in the current up to the third digit. More details of the simulation procedure can be found in Ref. [9]. Here we discuss the results from our investigations of single gate FD and dual-gate FD SOI devices.

III. SINGLE-GATE VS. DUAL-GATE DEVICES

The on-current degradation for different boundary conditions on the gate electrode in dual-gate devices is shown in Table I. In Tables II and III we show the corresponding current degradation for FD SOI devices with undoped/doped channel and different boundary conditions on the temperature of both the top and the bottom gate.

TABLE I
SIMULATION RESULTS FOR DUAL-GATE DEVICES

25nm DG SOI nMOSFET (Vgate-top=Vgate-bottom=1.2V; Vdrain=1.2V; Vsource=0V; Vsubstrate=0V)					
Type of simulation	Top gate temperature	Bottom gate temperature	Bottom of the BOX temperature	Current (mA/um)	Current decrease (%)
isothermal	300K	300K	300K	3.0682	\
thermal	300K	300K	300K	2.7882	**9.13**
thermal	400K	400K	300K	2.6274	**14.37**
thermal	600K	600K	300K	2.3153	**24.54**

$N_D=10^{19}$ cm^{-3}; $N_A=10^{11}$ cm^{-3}
t_{ox}=nm; t_{si}=12nm; t_{BOX}=50nm

TABLE II
SIMULATION RESULTS FOR FD-SOI DEVICES WITH UNDOPED CHANNEL

Type of simulation	*Gate temperature*	*Bottom of the BOX temperature*	*Current (mA/um)*	*Current decrease (%)*
isothermal	300K	300K	1.9428	\
thermal	300K	300K	1.7644	**9.18**
thermal	400K	300K	1.6641	**14.35**
thermal	600K	300K	1.4995	**22.82**

$N_D=10^{19}$ cm^{-3}; $N_A=10^{11}$ cm^{-3}
t_{ox}=2nm; t_{si}=10nm; t_{BOX}=50nm

TABLE III
SIMULATION RESULTS FOR FD-SOI DEVICES WITH DOPED CHANNEL

Type of simulation	*Gate temperature*	*Bottom of the BOX temperature*	*Current (mA/um)*	*Current decrease (%)*
isothermal	300K	300K	1.9290	\
thermal	300K	300K	1.8176	**5.78**
thermal	400K	300K	1.7467	**9.45**
thermal	600K	300K	1.5997	**17.10**

$N_D=10^{19}$ cm^{-3}; $N_A=10^{18}$ cm^{-3}
t_{ox}=2nm; t_{si}=10nm; t_{BOX}=50nm

We find that in dual gate devices there exists a larger bottleneck in temperature between the acoustic and optical

phonons (see Fig. 4) which causes about 4% more degradation in the current in this device structure when compared to the single gate structure. This is easily explainable with the fact that there are more carriers in the DG structure and the optical to acoustic phonon decay is not fast enough so that heating has more influence on the carrier drift velocity and, therefore, on-state current in dual-gate devices. In fact, we do observe larger degradation in the average carrier velocity in the dual-gate devices when compared to single FD SOI device structure (see Fig. 5).

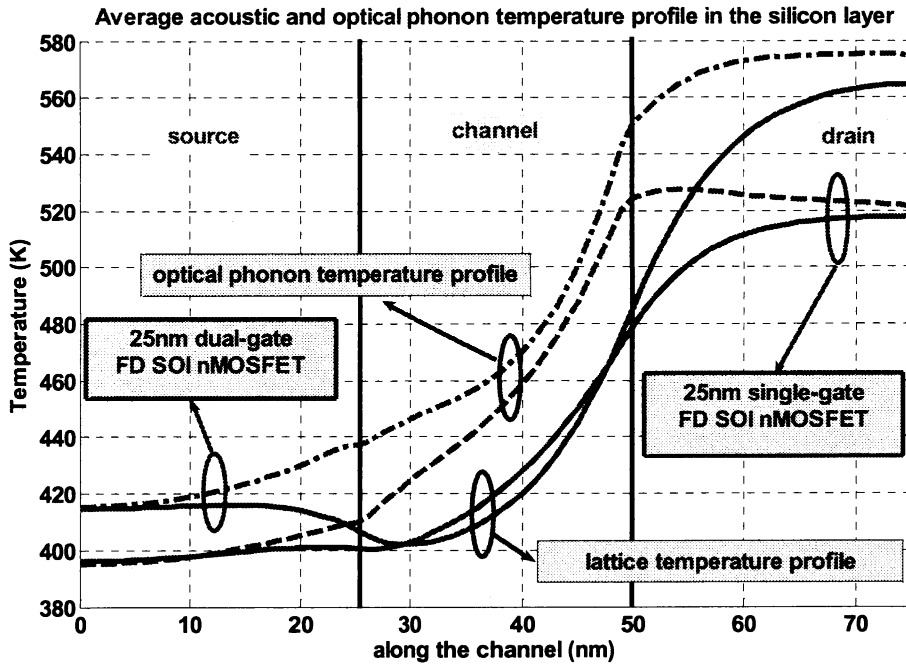


Fig. 4. Phonon Bottleneck in single gate (FD device) and dual gate structure.

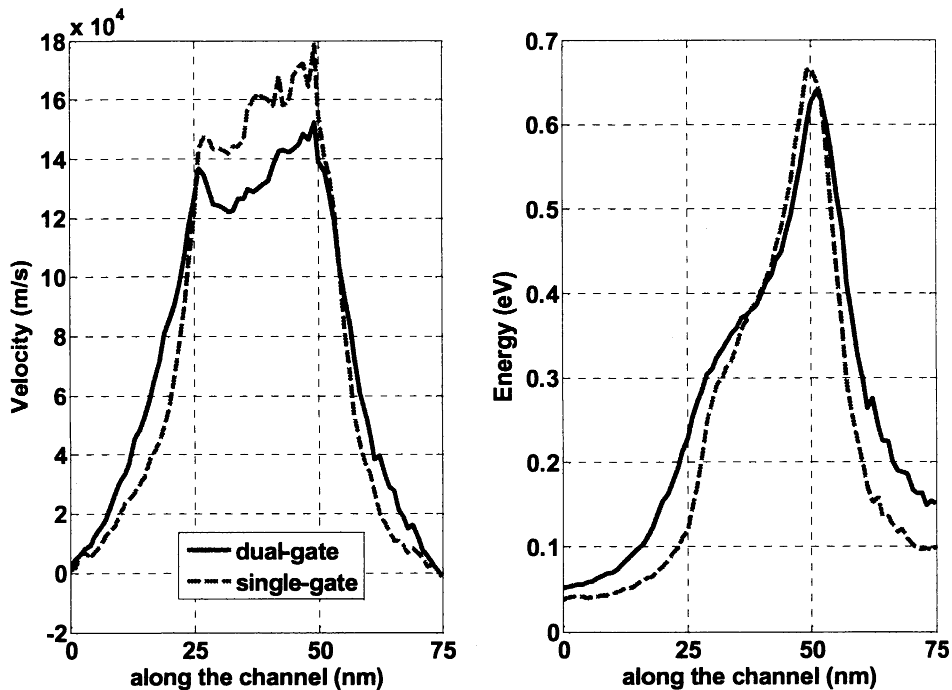
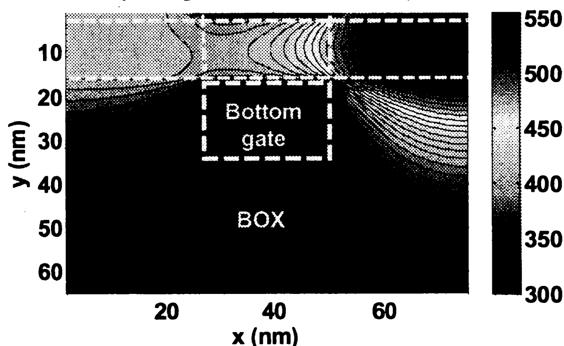
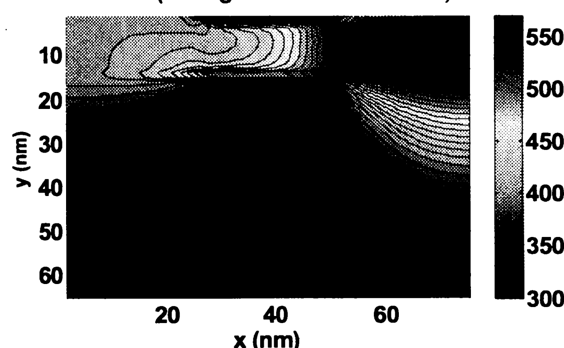


Fig. 5. Average carrier velocity (left panel) and average electron energy (right panel) along the channel.

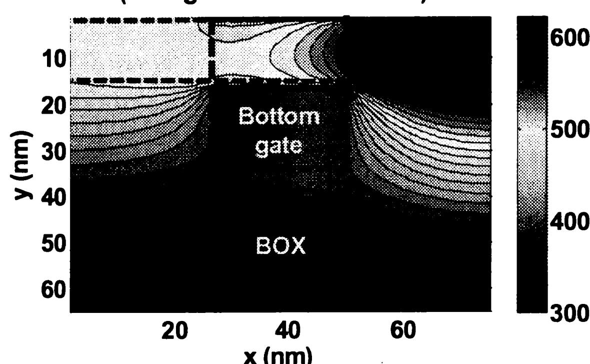
Lattice temperature profile for 25nm DG SOI MOSFET
(both gates are set to 300K)



Optical phonon temperature for 25nm DG SOI MOSFET
(both gates are set to 300K)



Lattice temperature profile for 25nm DGSOI MOSFET
(both gates are set to 400K)



Optical phonon temperature for 25nm DG SOI MOSFET
(both gates are set to 400K)

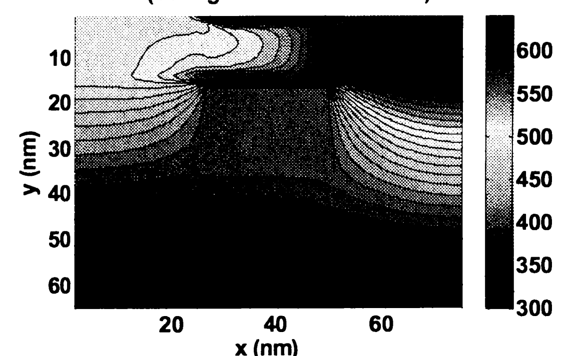


Fig. 6. Lattice and optical phonon temperatures for gate temperatures fixed to 300K and 400K.

The acoustic and optical phonon temperature maps for gate boundary conditions of 300K and 400K are shown in Fig. 6 for the dual-gate structure. Note that when increasing the boundary temperature on the gate, the hot spot moves more towards the channel. This is particularly pronounced for the optical phonon temperatures.

IV. Conclusions

In this work theoretical investigations have been performed regarding lattice heating in single gate FD and dual-gate devices. Our results suggest that the dual-gate structure is a structure of choice because of the following reasons. When we compare the current degradation of undoped channel dual-gate device and undoped channel FD SOI device, they are almost the same. There is about 5% decrease in the current degradation in the FD SOI device with doped channel. So, we might say that in the worst-case scenario, there is about 5% larger degradation in dual-gate devices due to lattice heating when compared to the optimized FD SOI devices. However, the magnitude of the on-current is 1.5-1.8 times larger in the dual-gate structure for the same bias conditions. Thus, one can trade off a slight increase in current degradation due to lattice heating for more current drive.

Acknowledgment

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