Progress in Modeling of SMT "Stress Memorization Technique" and Prediction of Stress Enhancement by a Novel PMOS SMT Process

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Abstract— **In this paper, we report progress in the modeling of stress memorization technique (SMT). We show that source/drain deformation plays a critical role in providing enhanced channel stress during SMT process. Stress enhancement as a function of the distance to gate edge of the amorphized source/drain regions is studied. We also propose a novel PMOS SMT process and demonstrate in simulation significant drive current gain additive to that of embedded SiGe process.**

Keywords: Stress, Stress Memorization Technique

I. INTRODUCTION

Stress engineering is vital to improve the performance of advanced CMOS technology. Stress memorization technique (SMT) is in wide use and effective for NMOSFET drive current enhancement. Since the first report of NMOSFET drive current improvement by a disposable stressor or capped poly process [1-2], stress memorization in poly gate and variations of such theory have been proposed to explain the enhanced channel stress absent of the initial stressor layer. Recently, SMT process at post NMOSFET source/drain (S/D) extension formation was also reported [3]. Even though qualitative explanation of SMT seems to capture correct trend, numerical modeling of such phenomena can be beneficial in providing quantitative physical understanding and thus enable optimization of the process. A stress memorization mechanism due to poly gate deformation during re-crystallization was proposed and numerically modeled by Adam *et al* at SISPAD 2005 [4]. In this paper, we extend the model to include both the S/D and poly gate re-crystallization processes. The deformation of the regions undergoing re-crystallization is modeled as a bilinear isotropic plastic process. Additionally, a novel SMT process is proposed to provide improved performance to PMOSFET. Significant PMOSFET performance gain is shown to be possible through numerical simulations

II. MODEL DESCRIPTION

A schematic illustration of the simulation methodology for NMOSFET is shown in Fig 1. The regions where stress memorization occur are amorphized before anneal. The amorphized regions, in both poly gate and S/D areas, are under initial stress from stressors, such as a capping layer. During annealing, the stressed regions undergo deformation during a re-crystallization process. This deformation process is simulated by a temperature-dependent plastic deformation model. Bilinear isotropic plasticity model is applied for the amorphized regions. During the cooling process, the plastic strain in the amorphized regions is mostly retained and the surrounding structure elastically conforms to those regions.

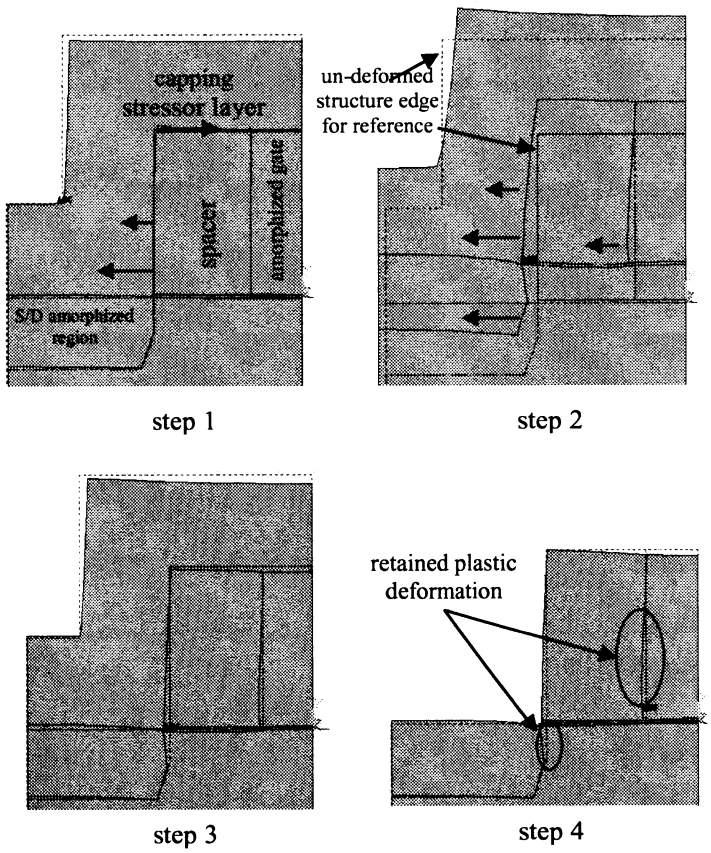


Fig. 1: Schematic illustration of steps of modeling SMT as a plastic deformation process (half structure shown and deformation is magnified by 15 X)

A well established mechanical stress simulator, ANSYS [5], is used to simulate the plastic deformation process and to calculate stress distribution. The material properties of silicon, polysilicon and the spacer material are obtained from reference [6], while the yielding stress and the hardening of the amorphized regions are treated as calibration parameters based on process details such as amorphization extent and re-crystallization temperature.

III. SIMULATION RESUTLS AND DISCUSSIONS

A. Post source/drain NMOSFET SMT

A silicon experiment of the post S/D SMT process is simulated. Fig. 2 compares the silicon process and the modeling flow. Only relevant steps are listed for comparisons to the stress modeling point of view. In order to model the amorphization, the material properties of S/D and poly regions are modified during lightly-doped extension (LDD) and S/D implantations. From wafer bowing measurements, the 400A thick capping stressor film is found to have ~600MPa initial tensile stress and an increased stress level of ~1.6GPa after anneal. This increase of stress is believed to be due to breaking of excess hydrogen bonds and releasing of moisture during the anneal process. This is modeled by loading 600MPa tensile stress into the capping stressor film as deposited and before the S/D anneal, then loading additional stress during temperature ramp to reach a final tensile stress level of 1.6GPa. During re-crystallization, the amorphous regions, such as LDD/SD and poly gate, deform, and this process is modeled by a bilinear plastic deformation process. The capping stressor film is removed after a 1050C RTA. Finally, a 400A and 1.6GPa tensile contact-etch stop liner (CESL) is deposited.

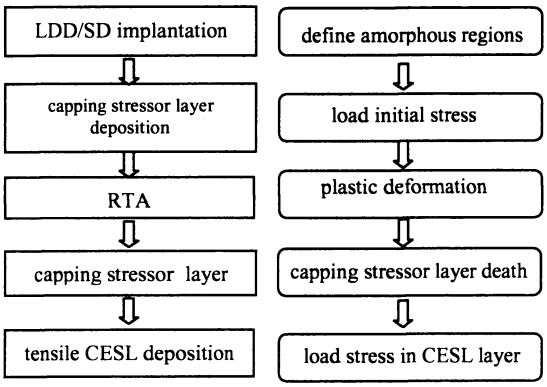


Fig. 2: Comparisons between process and modeling flows. Key relevant steps are listed

The material deformations at each step in the SMT process simulation are illustrated in Fig 1. It is noted that the deformation is magnified by 15 times in order to clearly show the shape change. At step 1, the initial stress of the capping stressor layer is loaded into the structure, which causes only elastic deformation. At step 2, after re-crystallization, plastic deformation in addition to elastic deformation can be seen in the poly gate and S/D regions. At step 3, the whole structure returns to an elastic state when cooled to room temperature, however, the plastic deformation is mostly retained in the poly gate and S/D regions. At step 3, the total deformation in the poly gate and S/D regions is clearly larger than that at step 1, due to the additional retained plastic deformation in these regions. At step 4, the capping layer removal is simulated using a material birth/death method. The retained deformations in the poly-gate and S/D regions then transmit stress into the channel. Based on the simulation results, the additional stress increase due to SMT is consistent with an observed drive current gain of ~10-15% from silicon experiment.

The SMT from poly gate and S/D regions are simulated separately in order to quantify contributions from each. As shown in Fig. 3, SMT in S/D and poly gate regions contribute nearly equally to the total drive current gain. It is also interesting to note that SMT in poly gate contributes more to the tensile stress along the channel direction, while SMT in S/D contributes effectively to the compressive stress vertically along the gate stack direction.

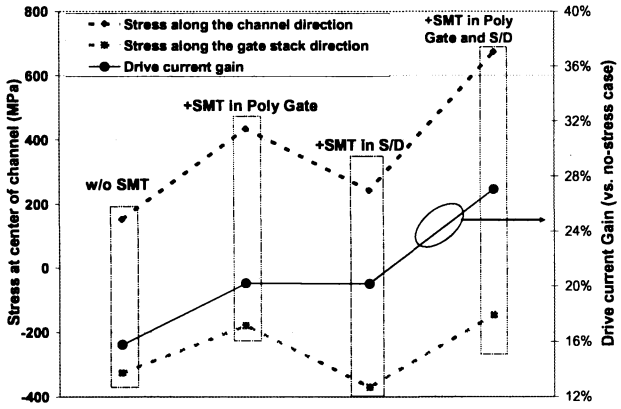


Fig. 3: Contributions to channel stress enhancement by poly gate and source/drain region SMT

In Fig. 4, simulated drive current gain as a function of location of the S/D amorphized regions relative to gate edge is plotted. It can be seen that further drive current gain from stress enhancement can be obtained if the S/D amorphized regions are moved closer to the gate edge. Simulation results show that an additional 5% drive current gain can be achieved if the S/D extension region is amorphized in addition to the deep S/D region. This is consistent with a literature report [3].

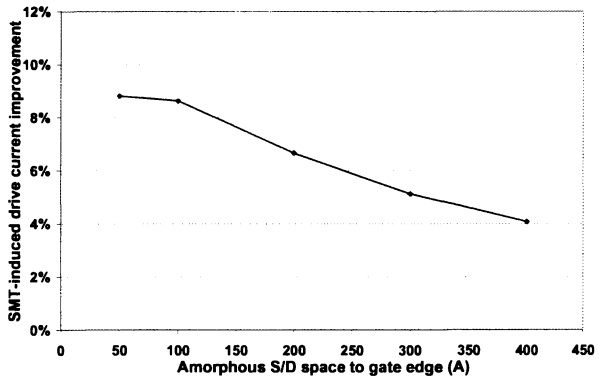
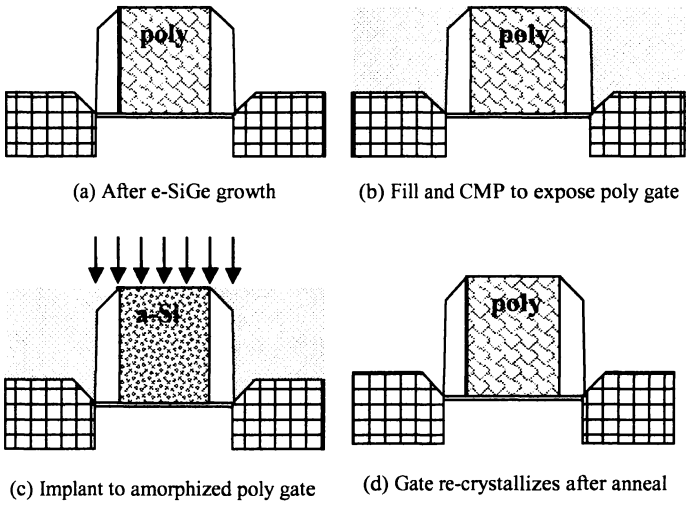


Fig. 4: Drive current enhancement as a function of distance between source/drain amorphization regions and gate edge

B. Novel SMT to enhance PMOSFET performance

We propose a novel process to provide PMOSFET performance improvement additive to that from embedded SiGe (e-SiGe). In this novel process, the PMOSFET poly gate is amorphized before S/D anneal. This process is schematically illustrated in Fig. 5. After e-SiGe growth, a protective layer is deposited over the whole wafer. A CMP process is then performed to expose the PMOSFET poly gate region. The poly gate is then amorphized through implantation. The protective layer is subsequently removed before S/D anneal. During the S/D anneal, the PMOSFET poly gate regions undergo re-crystallization and plastic deformation under the stress from e-SiGe. We show that the poly gate deformation in a PMOSFET with e-SiGe stressor can significantly increase PMOSFET channel stress and drive current.



(a) After e-SiGe growth (b) Fill and CMP to expose poly gate

(c) Implant to amorphized poly gate (d) Gate re-crystallizes after anneal

Fig. 5: Schematic illustration of a novel PMOSFET SMT process. During poly gate re-crystallization, the deformation of poly gate provides enhanced channel stress.

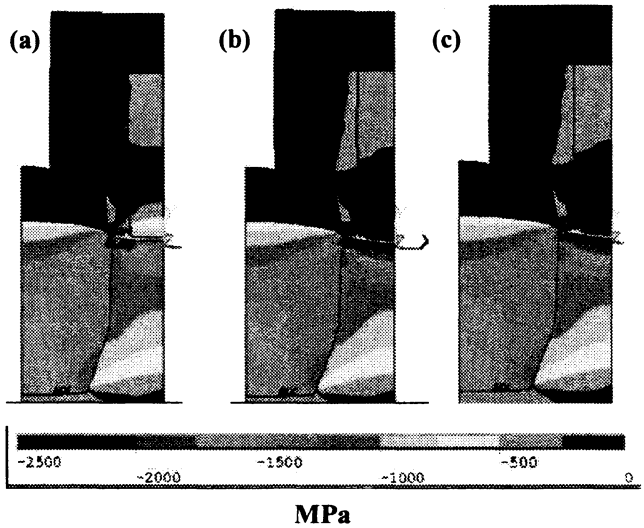
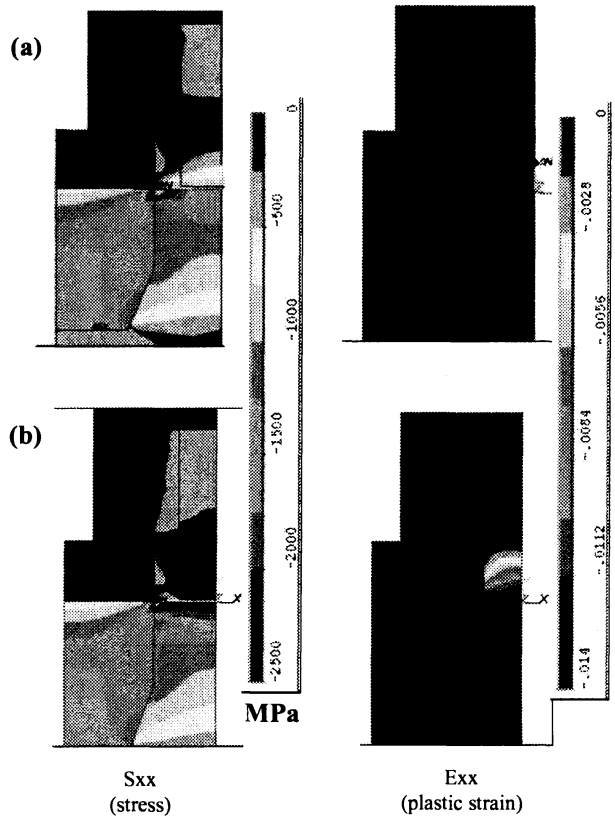


Fig. 6: Sxx, stress along the channel direction, at various steps of the PMOSFET SMT process: (deformation magnified 15X) (a) post e-SiGe growth (b) gate deforms during anneal (c) gate returns to elastic but retains deformation

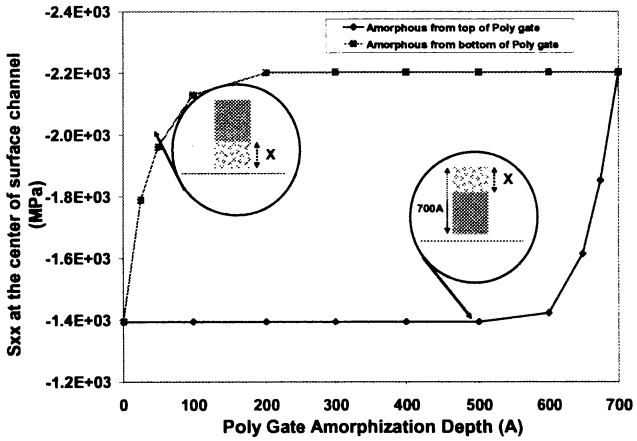
Stress distributions at various processing steps are plotted in Fig. 6. It is shown that the gate is further deformed during anneal and the additional deformation is memorized due to plasticity in poly gate at high temperature. Consequently the stress in the channel is enhanced. The stress and plastic strain distribution contours for eSiGe-only and eSiGe+SMT are compared in Fig. 7. It can be seen that the retained plastic deformation in the poly gate induces a channel stress increase by over 50%.



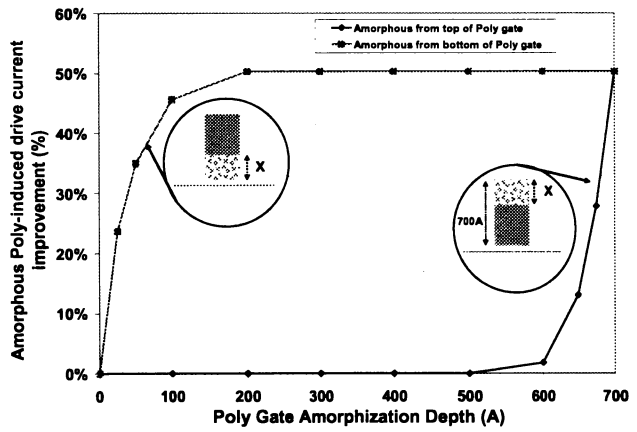
Sxx (stress) Exx (plastic strain)

Fig. 7: Comparison of stress and plastic strain along the channel direction for (a) e-SiGe only (b) e-SiGe+poly gate SMT

Fig. 8 (a) and (b) show the channel stress enhancement and drive current gain as a function of amorphization depth of the PMOSFET poly gate. It is found that the deformation of the first 10nm of the poly gate directly above gate oxide makes the most contribution to the channel stress enhancement. In this case, the additional stress from plastic deformation in poly gate can be most effectively transmitted into the Si channel. Depending on the extent of poly gate amorphization, drive current gain ranging from 10% to over 50% can be attained. Compared to the dual stress liner process [7], this proposed novel PMOSFET SMT is more scalable to smaller pitches.



(a)



(b)

Fig. 8: (a) Channel stress vs. X (poly-gate amorphization depth) (b) additional drive current gain over e-SiGe without SMT vs. amorphization depth

IV. CONCLUSIONS

We report progress in numerical modeling of the stress "memorization" effect. For the NMOSFET post S/D SMT process with disposable capping stressor layer, the simulations confirm that deformation in the amorphized S/D regions make significant contribution to channel stress enhancement. If S/D extension amorphization is included in SMT process, the simulations show that additional channel stress enhancement can be obtained. We also propose a novel PMOSFET SMT process with e-SiGe and predict significant channel stress and 10~50% performance enhancement.

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