

# Band-engineering of Novel Channel Materials for High Performance Nanoscale MOSFETs

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**Abstract**— In order to continue the scaling of silicon-based CMOS and maintain the historic progress in information processing and transmission, innovative device structures and new materials have to be created. A channel material with high mobility and therefore high injection velocity can increase on current and reduce delay. Currently, strained-Si is the dominant technology for high performance MOSFETs and increasing the strain provides a viable solution to scaling. However, looking into future scaling of nanoscale MOSFETs it becomes important to look at higher mobility materials, like Ge and III-V materials together with innovative device structures and strain, which may perform better than even very highly strained Si. For both Ge and III-V devices problems of leakage need to be solved. Novel heterostructure quantum-well (QW) FETs will be needed to exploit the promised advantages of Ge and III-V based devices.

Tunneling (BTBT) (including bandstructure and quantum effects) simulations, the effect of uniaxial- and biaxial-strain, band-structure, mobility, effective masses, density of states, channel orientation and high-field transport on the drive current, off-state leakage and switching delay in nano-scale, Si, SiGe and Ge, p-MOS DGFETs (Fig. 1) was thoroughly and systematically investigated [3, 4].

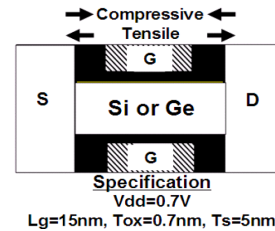


Figure 1. Specification of the Nanoscale DGFET used in this study

## I. INTRODUCTION

It is well accepted that below the 32-nm node although the conventional Si CMOS can be scaled, performance gains will be sharply diminished. A channel material with high mobility ( $\mu$ ) and therefore high injection velocity ( $v_{inj}$ ) can increase  $I_{ON}$  and reduce delay and thus allow continued scaling [2, 3]. Currently, strained-Si is the dominant technology for high performance MOSFETs and increasing the strain provides a viable solution to scaling. However, looking into future scaling of nanoscale MOSFETs it becomes important to look at higher mobility materials, like Ge and III-V together with innovative device structures and strain, which may perform better than even very highly strained Si. In this work we assess the performance of Si, Ge, and III-V materials like GaAs, InAs and InSb, which may perform better than even very highly strained-Si.

## II. GE MOSFETS

### A. Strain Engineered Ge p-MOSFETs

Strain engineering in Ge can significantly increase  $\mu_p$  because of a reduction in  $m^*$  and the band splitting due to strain [3]. In extremely scaled p-MOSFETs, the relation between the short-channel drive currents ( $I_{ON}$ ) and mobility ( $\mu_p$ ) is neither direct nor obvious. Using the Non-local Empirical Pseudopotential method (bandstructure), Full-Band Monte-Carlo Simulations (transport), 1-D Poisson-Schrodinger (electrostatics) and detailed Band-To-Band-

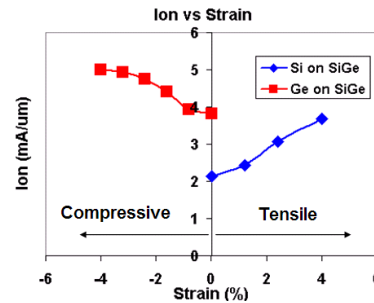


Figure 2. Drive current enhancements are largest for compressive biaxially s-Ge. Relaxed Ge shows higher drive than biaxially s-Si due to lower transport mass and higher DOS.

Fig. 2 shows  $I_{ON}$  enhancement vs different biaxial strain for the nanoscale DGFET structure ( $T_s=5\text{nm}$ ,  $L_g=15\text{nm}$ ,  $T_{ox}=0.7\text{nm}$ ,  $V_{dd}=0.7\text{V}$ ). For biaxial strain, clearly, the highest drive currents are obtained in highly strained-Ge. Even though, strained-Si has a very high ( $\sim 2.5X$ ) low-field mobility, even relaxed-Ge performs better because of its lower transport mass and higher DOS. The overall transport is still strongly dominated by high-field transport. The minimum possible (BTBT limited) off-state leakage achievable is shown in Fig. 3. Due to its extremely small bandgap, highly strained-Si exhibits a very large leakage. Unlike Si, the leakage with strain for strained-Ge is not monotonic and shows an optimum at  $\sim 1.3\%$  compressive biaxial strain. With strain, due to the increase in the  $\Gamma$ -valley the leakage initially reduces but then due to the rapid reduction in the X-valley, the leakage again increases. For biaxial strain,  $\sim 2\%$  strained-Ge provides the best trade-off between lower leakage ( $\sim 10\text{nA}$ ) and drive current enhancement / delay reduction ( $\sim 2.5X$ ).

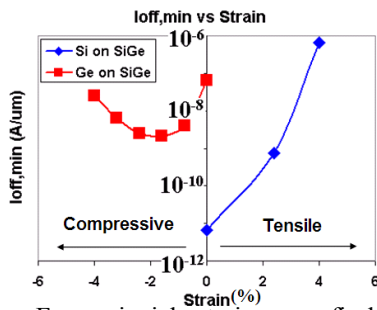


Figure 3. The minimum achievable (BTBT limited) off-state leakage is worst for highly s-Si, due to its small bandgap. Ge shows an initial reduction in leakage by  $\sim 10X$  with strain due to the increase in the direct  $\Gamma$ -valley bandgap.

For uniaxial strain, we find that the large velocity overshoot in compressive Si [110] leads to very high drive currents (Fig. 4). The higher mobility of Ge [100] and the higher velocity of Ge [110] compensate, leading to very similar drive currents, which are the highest among all the channels/strain considered. The minimum off-state leakage in compressive Ge [110] is an order of magnitude lower than Ge [100] because of its larger L- and  $\Gamma$ -valley bandgaps and tunneling mass (Fig. 5). Si [110] shows the lowest leakage, ( $\sim 2$  orders lower than Ge), due to its large indirect X-valley bandgap. For uniaxial strain of about 1 GPa, compressively strained-Ge [110] or Ge [100] perform the best in terms of drive current enhancement/delay reduction ( $\sim 3.5X$ ), but this comes with a penalty of increased off-state leakage.

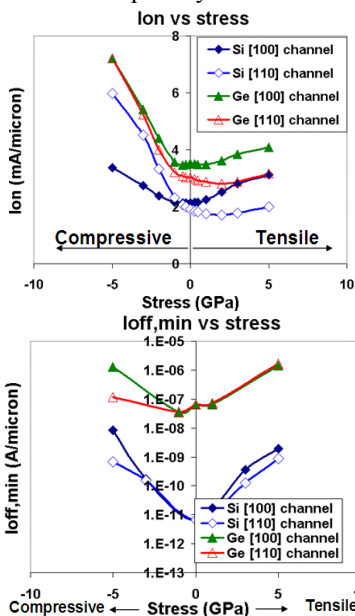


Figure 4. The drive current for Ge [100] and Ge[110] under uniaxial compressive stress is greatly enhanced (3.5X). Si[110] also shows very high drive current (2.5X) due to enhanced high field transport and strongly anisotropic effective mass.

Figure 5. The minimum achievable off-state leakage for [110] under compressive stress is lower than [100] for Si and Ge because of the larger bandgap. Si [110] shows the lowest leakage.

### B. Quantum-Well (QW) Heterostructure Strained-Ge p-MOSFETs

Strain in general results in reduction in the  $E_G$  and hence enhanced off-state leakage ( $I_{BTBT}$ ). Confinement on the other hand results in increased  $E_G$  as shown in Fig. 6, and hence reduces  $I_{BTBT}$ . The heterostructure QW-FET of Fig. 7 proposes a unique and novel device structure to combine strain and quantum mechanical confinement to obtain desired transport properties with reduced off-state leakage [5-8]. In these structures the transport can be confined to the center of the channel in a high mobility material flanked by a high  $E_G$  material. The Si capping layer helps in providing a very good high-k gate dielectric interface and reduced mobility degradation due to interface states. The mobility is further

enhanced due to strain, reduced electric field in the center of the double gate structure due to symmetry and the channel being away from the dielectric interface. The bandgap of the center channel can be increased due confinement by keeping it very thin.

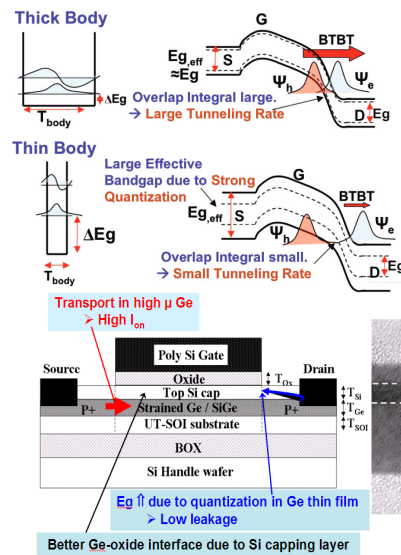


Figure 6. Quantum-well with ultra-thin body leads to strong confinement, which increases the effective bandgap and lowers the tunneling rate.

Figure 7. Schematic of s-Ge Quantum Well (QW) heterostructure MOSFETs (H-FET) on SOI substrates, exhibiting high drive currents and low off-state leakage. Cross-sectional TEM of defect free ultra-thin strained Ge Quantum Well epitaxially grown on a relaxed SOI substrate.

We have demonstrated [5-8] a novel Si/s-Ge/Si heterostructure QW-FET, in which the transport occurs in high  $\mu_p$  s-Ge quantum well and leakage in the wider  $E_G$  Si (Fig. 7). This structure reduces the  $I_{BTBT}$ , while retaining high  $\mu_p$  of Ge. The confinement of thin Ge between Si results in an increase in the  $E_G$  and hence reduction in  $I_{BTBT}$ , while strain keeps  $\mu_p$  high. Experimentally, the resulting optimal structure obtained was an ultra-thin (2nm), low defect, fully strained Ge epi-grown quantum-well channel on relaxed bulk-Si (r-Si). QW-FETs on bulk Si show a  $\sim 2X$   $\mu_p$  enhancement over Si, while QW-FETs on SOI show even higher  $\mu_p$  enhancements of  $>4X$  over Si (Fig. 8). Both types of QW-FETs show reduction in  $I_{OFF}$  compared to bulk Ge devices. In particular QW-FETs on SOI show a significant reduction in  $I_{OFF}$  due to the reduced E-field in Ge and the effective bandgap increase due to confinement (Fig. 9).

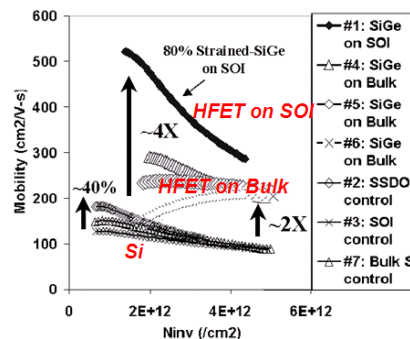


Figure 8. Experimental hole mobility vs.  $N_{inv}$  for different QW H-FET device structures with different strained-SiGe channels.

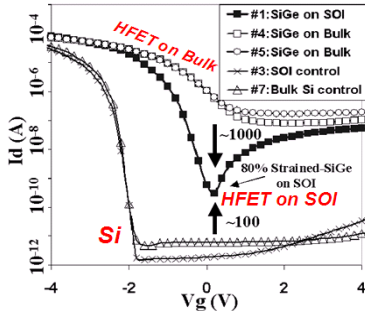


Figure 9. Experimental  $I_d$ - $V_g$  characteristics of the s-Ge QW H-FETs showing reduction in leakage and good electrostatic control. It has a degraded subthreshold slope due to the thicker gate oxide used in this study and the Ge-related defects at the interface, which can be improved

However, QW FETs are not completely free from their tradeoffs. SG QW FETs are found to have dramatic mobility degradation at QW thickness of less than  $\sim 4$ nm due to strong quantum confinement effects [10]. Theoretical optimums obtained through simulations of the mobility, drive current and delay, in highly scaled s-Ge QW DG FETs ( $L_g=15$ nm,  $T_s=5$ nm), suggest an optimum QW thickness of  $\sim 2$ nm [9].

### III. III-V MOSFETs

On an initial glance, due to their extremely small transport mass leading to high injection velocity ( $v_{inj}$ ), III-V materials appear to be very attractive candidates as channel materials for highly scaled n-MOSFETs [11-13]. However, III-V materials have many significant and fundamental issues, which may prove to be severe bottlenecks to their implementation. These tradeoffs need to be systematically and thoroughly investigated from a theoretical standpoint in order to help in providing useful guidelines, which can efficiently streamline the resources invested by several research groups throughout the world in their experimental development.

#### A. Benchmarking III-V Materials (GaAs, InAs, InP, InSb)

Although their small transport mass leads to high injection velocity ( $v_{inj}$ ), III-V materials have a low density of states (DOS) in the  $\Gamma$ -valley, tending to reduce the inversion charge ( $Q_{inv}$ ) and hence reduce drive current [14-18]. Furthermore, the small direct band gaps of Ge and III-V materials inherently give rise to very large band to band tunneling (BTBT) leakage current compared to Si [19]. They also have a high permittivity and hence are more prone to short channel effects (SCE). Quantum confinement in these ultra-thin nanoscale DGFETs plays a very important role. In III-V materials, large quantum confinement makes electrons populate and conduct in heavier L- or X-valleys. Furthermore, there is a significant increase in the conductivity mass in quantized sub-bands due to large non-parabolicity of  $\Gamma$ -valley [18, 20]. Quantum confinement effects also reduce BTBT leakage in ultra thin channel [19]. In a theoretical study, we have thoroughly investigated Double Gate (DG) n-MOSFETs with Ge and III-V materials (GaAs, InP,  $In_xGa_{(1-x)}As$ , InAs and InSb) and compared to Si [20]. The simulations performed under ballistic transport take into account non-parabolic full band structure, quantum confinement effects, BTBT leakage and SCE effects. Device structure and bias conditions are  $L_G=15$ nm,  $T_{OX}=0.7$ nm,  $T_s=3-10$ nm and  $V_{DD}=0.3-0.7$ V. Source and drain are assumed to be perfect absorbers.

Despite of low inversion charge ( $Q_{inv}$ ), thanks to their large injection velocity ( $v_{inj}$ ), III-V materials like InAs, InSb and

InP can flow up to 80% larger drive current than Si. The  $I_{OFF,BTBT}$  in Ge, InAs, GaAs and InSb can be reduced by over  $\sim 1000$ X by scaling  $T_s$  to 3nm (Fig. 10), due to enlarged bandgap by quantization of sub-bands. In GaAs majority of electrons reside in L-valleys, which makes GaAs behave like Ge but with slightly worse  $I_{ON}$ . Intrinsic delay is strongly dependent on transport effective mass, thus III-Vs always switch faster than Si by up to  $\sim 6$ X (Fig. 11). Small bandgap materials such as InAs, InSb and Ge have extremely large  $I_{OFF,BTBT}$  higher than  $0.1\mu A/\mu m$ . Scaling  $T_s$  enhances the device performance by eliminating the SCE effect and reducing BTBT leakage. Overall, among all the unstrained III-V materials  $In_{0.25}Ga_{0.75}As$  and InP exhibit the best performance - high  $I_{ON}$ , low delay and low  $I_{OFF,BTBT}$  compared Si. Ge has highest  $I_{ON}$  due to its large DOS and small transport effective mass, but it suffers from large BTBT leakage.

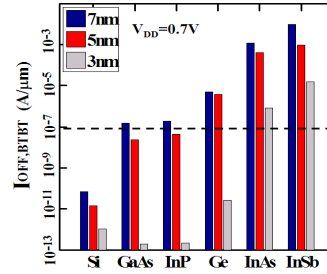


Figure 10.  $I_{OFF,BTBT}$  for various  $T_s$ . Scaling of  $T_s$  reduces  $I_{OFF,BTBT}$  effectively, since the quantum confinement effect reduces BTBT. Small bandgap materials such as Ge, InAs, InSb suffer large  $I_{OFF,BTBT}$ . Larger than  $\sim 1000$ x reduction is observed in GaAs, InP and Ge by scaling  $T_s$  from 10nm to 3nm

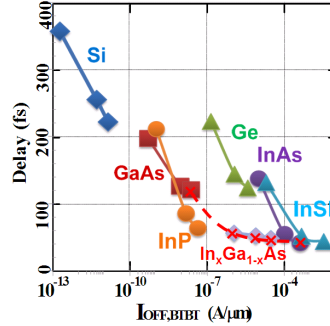


Figure 11. Intrinsic delay vs  $I_{OFF,BTBT}$  trade-off in various materials.  $L_g=15$ nm,  $T_{OX}=0.7$ nm,  $T_s=5$ nm. Si exhibits slowest switching and lowest  $I_{OFF,BTBT}$ . Although delays for InAs and InSb are small, they suffer extremely large  $I_{OFF,BTBT}$ . InGaAs and InP exhibit fast switching times and large  $I_{ON}$  at reduced  $I_{OFF,BTBT}$

#### B. Strain Engineered III-V Materials ( $In_xGa_{1-x}As$ )

Just like in the case of Si or Ge, strain engineering can be used to further enhance the performance in III-V materials in terms of both, increasing the drive current and reducing the off-state leakage. In another simulation study [21, 22], the performance of uniaxial- and biaxial- strained  $In_xGa_{1-x}As$  NMOS Double Gate FETs (DGFET) with (111) and (001) orientations were thoroughly investigated under ballistic transport, taking into account non-parabolic full band structure, quantum effects, band-to-band tunneling (BTBT) and short-channel effects (SCE). The real and complex band structures for different composition, uniaxial and biaxial (tensile and compressive) strain are calculated using the local empirical pseudopotential method (LEPM). In this work, by varying strain conditions and orientations for the different materials, the best performing strained  $In_xGa_{(1-x)}As$  materials were identified.

$In_xGa_{1-x}As$  is a very promising candidate for future n-FETs. The main factors affecting the performance of the III-V materials, are the  $m_{eff}$ ,  $\Gamma$ -L valley separation ( $\Delta E_{\Gamma-L}$ ),  $E_g$  and  $m_{Tunnel}$ . Based on our simulation results, GaAs(001),  $In_{0.25}Ga_{0.75}As(001)$  and  $In_{0.75}Ga_{0.25}As(111)$  are selected as the



best channel materials. Fig. 13 depicts the best channel materials and how they can be improved by strain engineering. GaAs(001) has lowest  $I_{OFF,BTBT}$  due to its large bandgap ( $>1.4\text{eV}$ ). With the biaxial tensile strain, GaAs(001) can have  $I_{ON}$  as high as InGaAs, since the strain increases  $\Delta E_{\Gamma-L}$  (Fig. 12) with marginal increase in  $I_{OFF,BTBT}$ .  $\text{In}_{0.25}\text{Ga}_{0.75}\text{As}(001)$  exhibits both good  $I_{ON}$  and low  $I_{OFF,BTBT}$  because of its large bandgap ( $>1\text{eV}$ ) and large  $\Delta E_{\Gamma-L}$ . The leakage in  $\text{In}_{0.25}\text{Ga}_{0.75}\text{As}(001)$  can be further reduced with 4% uniaxial compressive strain, without significant reduction in  $I_{ON}$ .  $\text{In}_{0.75}\text{Ga}_{0.25}\text{As}(111)$  has excellent carrier transport properties, but it suffers large  $I_{OFF,BTBT}$ . Biaxial compressive strain can reduce the leakage in  $\text{In}_{0.75}\text{Ga}_{0.25}\text{As}(111)$  below  $0.1\mu\text{A}/\mu\text{m}$ . Considering future scaled devices with thinner body,  $\text{In}_{0.75}\text{Ga}_{0.25}\text{As}(111)$  may be the best material. Larger quantization effect in thinner body will further increase the bandgap of  $\text{In}_{0.75}\text{Ga}_{0.25}\text{As}(111)$ , leading to even smaller leakage current. In contrast, for GaAs(001) and  $\text{In}_{0.25}\text{Ga}_{0.75}\text{As}(111)$ , the quantization effect will result in a penalty of lower  $I_{ON}$  due to reduction of  $\Delta E_{\Gamma-L}$ . At a  $100\text{nA}/\mu\text{m}$   $I_{OFF}$  specification, 4% biaxial compressive strained  $\text{In}_{0.75}\text{Ga}_{0.25}\text{As}(111)$  NMOS DGFET outperforms other InGaAs compositions because of the excellent transport properties and reduced leakage current with strain engineering.

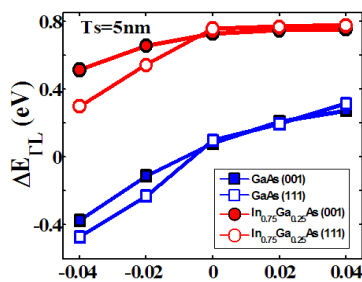


Figure 12.  $\Gamma$ -L Separations as a function of strain ( $\epsilon_{11}$ ) in 5nm film. Tensile strains widen the separation. With tensile strain,  $\Delta E_{\Gamma-L}$  in GaAs can be over 0.3 eV

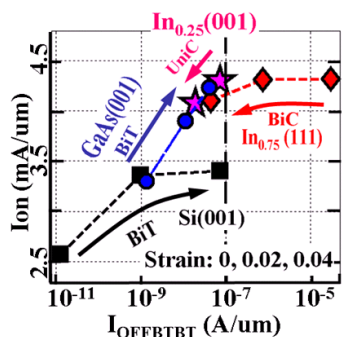


Figure 13.  $I_{ON}$  and  $I_{OFFBTBT}$  of the best performing n-DGFETs with materials, biaxial strained GaAs (001), uniaxial compressive strained  $\text{In}_{0.25}\text{Ga}_{0.75}\text{As}(001)$  and biaxial compressive strained  $\text{In}_{0.75}\text{Ga}_{0.25}\text{As}(111)$ . Strain levels are 0, 0.02 and 0.04. Values for biaxial tensile strained Si are given for comparison

To take complete advantage of high mobility III-V materials, heterostructure quantum-well FETs, which can simultaneously achieve high drive currents and low off-state leakage should be investigated, similar to the case of Ge [5, 6].

#### IV. CONCLUSION

MOSFETs utilizing high mobility Ge and III-V channel materials can take us to the sub-20 nm regime. Ge with strain engineering will be suitable to satisfy the p-MOS requirements. However, there appear to be severe practical limitations in case of n-MOS. High mobility III-V materials, such as  $\text{In}_x\text{Ga}_{(1-x)}\text{As}$  with strain engineering could be suitable for n-MOS. However, to take full advantage of high mobility/small bandgap channel materials, novel device

structures, such as heterostructure quantum well (QW) FETs along with strain engineering will be needed, in order to achieve high drive currents while maintaining low off-state leakage. For these materials to become mainstream, important challenges, such as, good surface passivation, low parasitic resistance, and heterogeneous integration on Si platform must be overcome.

#### ACKNOWLEDGMENTS

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