Understanding and Engineering of Carrier Transport in Advanced MOS Channels

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***Abstract*— Mobility enhancement technologies have currently been recognized as mandatory for future scaled MOSFETs. In this paper, we review the basic concept on the choice of channel materials for high performance MOSFETs and address several important issues on carrier transport properties of mobility-enhanced CMOSFETs, including the effects of uniaxial strain on Si n-MOSFETs and the critical issues on Ge/III-V MOSFETs.**

Keywords-MOSFETs, channels, subband, mobility, velocity, strain, Ge, III-V semiconductors, scattering

I. INTRODUCTION

It has been well recognized that, under sub-100 nm regime, conventional device scaling concept has confronted with several physical and essential limitations. Therefore, any new device engineering to realize advanced CMOS by overcoming these difficulties is strongly needed. A group of theses new device technologies called the technology boosters can be classified mainly into three categories, as schematically shown in Fig. 1, gate stack engineering, source engineering and channel engineering [1]. Particularly, the channel engineering includes carrier-transport-enhanced channels aiming at high current drive and multi-gate channels aiming at high immunity for short channel effects. Among them, the carrier-transport-enhanced channels are recently becoming more important. Recently, other channel materials than Si have also stirred strong interests from the viewpoint of ballistic transport.

This paper briefly reviews the requirements of these materials as channels for high current drive MOSFETs. Also, the critical issues for realizing these MOSFETs are discussed in terms of the carrier transport.

II. OPTIMUM DESIGN OF PHYSICAL PARAMETERS OF CHANNEL MATERIALS

A. *Mobility and Effective Mass Engineering* [2]

The drive current of MOSFETs per gate width can be simply represented by $I_{on} \approx qN_s^{source} \cdot v_s$, where q is the elemental charge, N_s^{source} is surface carrier concentration near source edge and υ_s is carrier velocity near source edge [3]. As the channel length becomes shorter, non-stationary transport becomes more dominant, where sufficient numbers of scattering events do not occur inside the channels. This situation has been formulated as quasi-ballistic transport by Lundstrom [3, 4] and has been quantitatively analyzed in detail by many research groups [5-7]. Here,

$$I_{on} = qN_s^{source} \cdot v_{inj} \cdot \frac{1-r}{1+r} \quad (1)$$

where υ_{inj} is injection velocity at the top of the barrier near the source edge and r is back scattering rate near source region. Since r is directly related to μ_s, the enhancement of mobility can be still important in increasing I_{on} under quasi ballistic transport regime.

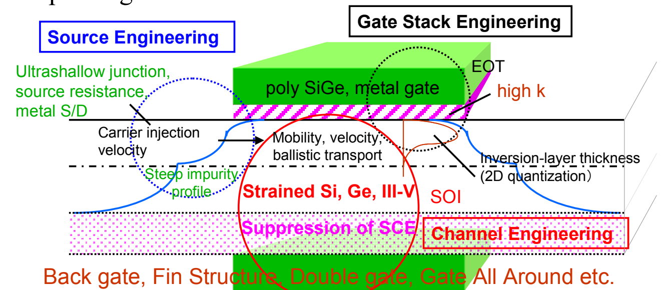

Fig. 1 Schematic diagram of three types of device engineering

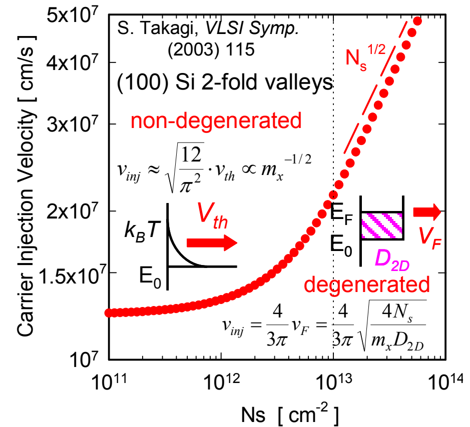

Fig. 2 Calculated injection velocity as a function of N_s

Furthermore, when channel length becomes much shorter, probably down to less than 10 nm in Si MOSFETs [6], and no carrier scattering events occur inside the channel, the carrier transport is dominated by full ballistic transport. Here, I_{on} in MOSFETs under this ballistic transport, which have also been formulated by Natori [8, 9], is simply represented by

$$I_{on} = qN_s^{source} \cdot v_{inj} \quad (2)$$

Thus, the enhancement of υ_{inj} is necessary to increase I_{on} of ballistic MOSFETs. Fig. 4 shows the calculated values of υ_{inj} for electrons in the 2-fold valleys on a (100) Si surface at

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room temperature as a function of N_s [10]. An important point is that υ_{inj} in both low N_s region (thermal velocity) and high N_s region (Fermi velocity) increases with a decrease in m_x and, thus, the reduction in the effective mass along the current flow direction is a key in enhancing υ_{inj} and resulting I_{on} under ballistic transport.

It has been recognized, however, that the reduction in the effective mass or, more essentially, the reduction in D_{2D} can reduce I_{on} under a fixed value of V_g through a different mechanism. This is because the reduction of the effective mass reduces inversion-layer capacitance, C_{inv}, and resulting C_g [11]. Here, it is also known [12, 13] that C_{inv} is determined by two components, the inversion-layer capacitance due to finite density-of-states, C_{inv}^{DOS}, and the inversion-layer capacitance due to quantum mechanical thickness of inversion layers, $C_{inv}^{thickness}$. The total C_{inv} can be represented by the series capacitance of these two capacitances. Under an assumption of single subband occupation, C_{inv}^{DOS} and $C_{inv}^{thickness}$ for 2D carriers can be described as follows,

$$C_{inv}^{DOS} = q^2 \cdot D_{2D}(1 - \exp(-qN_s/D_{2D})) \quad (3)$$

$$C_{inv}^{thickness} \approx \frac{\varepsilon_s}{W_{inv}} = m_z^{1/3} \cdot \left(\frac{4\varepsilon_s^2 q^2}{9\hbar^2}\right)^{1/3} \cdot \left(N_{dpl} + \frac{11}{32}N_s\right)^{1/3} \quad (4)$$

where ε_s, W_{inv}, m_z, N_{dpl} are the permittivity of semiconductors, effective thickness of inversion layers, the effective mass normal to MOS interfaces and surface space charge concentration, respectively. As a result, C_{inv}^{DOS} is determined by m_x, m_y and n_v, while $C_{inv}^{thickness}$ is determined by m_z. When D_{2D} becomes significantly lower with smaller values of m_x, m_y or n_v, C_{inv}^{DOS} dominates C_{inv} in the entire N_s region.

In order to obtain higher C_g and N_s, larger C_{inv} is favorable, meaning that heavier m_x, m_y and m_z and larger n_v can yield higher N_s under given values of T_{ox} and V_g. However, heavier m_x directly reduces υ_s and the increase in D_{2D} causes the increase in the scattering probability of 2D carriers and the resulting increase in r, meaning that the optimum values of m_x, m_y and n_v to maximize I_{on} can be determined from the trade-off relationship between N_s^{source} and υ_s. It should be noted here that the impact of C_{inv} on I_{on} is dependent on T_{ox}. For thicker T_{ox}, the effect of the effective mass on υ_s is more evident and, thus, lower values of m_x, m_y and n_v result in higher I_{on}. For thinner T_{ox}, the effect of the effective mass on C_{inv} is more evident and, thus, appropriately high values of m_x, m_y and n_v are favorable.

As a result, the guidelines for enhancing I_{on} by the effective mass are summarized as follows.

(1) Heavier m_z for reducing the inversion-layer thickness and increasing $C_{inv}^{thickness}$.

(2) Lighter m_x for increasing υ_s.

(3) Optimized D_{2D} in thin T_{ox} from the viewpoint of the trade-off between C_{inv}^{DOS} and υ_s.

(4) $m_y > m_x$, in particular, for thinner T_{ox} and shorter L_g, where lighter m_x is better under a given value of D_{2D}.

B. Choice of Channel Materials

Table 1 lists the bulk electron and hole mobility, the electron and hole effective mass, the band gap and the permittivity of Si, Ge and main III-V semiconductors. It is confirmed that the electron mobility of the III-V materials is quite high. Since this high mobility is basically attributed to the light effective mass, we can expect high υ_{inj} in these materials. GaAs and InP have larger bandgap that Si and Ge, which is suitable for low power applications.

Table 1. Mobility, effective mass and bandgap of electrons and holes in principal semiconductors

	Si	Ge	GaAs	InP	InAs	InSb
Electron mob. (cm^2/Vs)	1600	3900	9200	5400	40000	77000
Electron mass (/m_0)	mt: 0.19 ml: 0. 916	mt: 0.082 mt: 1.467	0.067	0.082	0.023	0.014
Hole mob. (cm^2/Vs)	430	1900	400	200	500	850
Hole mass (/m_0)	m_{HH}: 0.49 m_{LH}: 0.16	m_{HH}: 0.28 m_{LH}: 0.044	0.45 0.082	0.45 0.12	0.57 0.35	0.44 0.016
bandgap (eV)	1.12	0.66	1.42	1.34	0.36	0.17

Table 2. Ways to enhance carrier transport properties in MOS channels

	nMOSFET	pMOSFET
Channel Direction	-	<100> on (100) <110> on (110)
Surface Orientation	(100)	(110)
Strain in Si/Ge	biaxial or uniaxial tensile	biaxial tensile or uniaxial compressive
Materials	III-V	SiGe/Ge

As for the hole transport, on the other hand, Ge is known to provide the highest hole mobility among the main semiconductors. Also, it has actually been demonstrated that compressively-strained Ge p-MOSFETs provide 10 time or higher hole mobility against Si p-MOSFETs [14, 15]. Thus, Ge-channel MOSFETs have also been regarded as one of the most promising channel materials for high speed application. It is also well recognized that uni-axial compressive strain is quite effective in boosting the hole transport in Si MOS inversion layers [16], which has been explained from the viewpoint of both the effective mass modulation and the band splitting [17-19]. Table 2 summarizes the existing approaches to enhance the drive current of n- and p-MOSFETs through the choices of channel directions, surface orientations, strain applications and channel materials.

III. STRAINED-SI TECHNOLOGIES FOR ADVANDEC CMOS STRUCTURES

One of main effects of strain on n-MOSFET performance is based on the modulation of the occupancy of electrons in the subbands. The basic concept of the mobility enhancement in n-MOSFETs on (100) and (110) surfaces is schematically shown in Fig. 3. It is well known that tensile strain is effective in mobility enhancement on (100). As for (110), the optimum strain configuration is dependent on the channel direction. While biaxial tensile strain or uniaxial tensile strain along <100> is favorable for channels along <100> [20], uniaxial tensile strain along <110> is favorable for channels along

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<110> [21, 22], according to the considerations on the anistropic effective mass of Si.

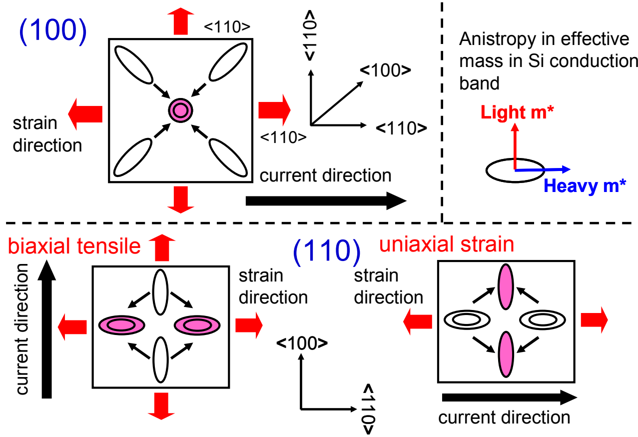


Fig. 3 Schematic diagram of effects of strain on the subband occupation

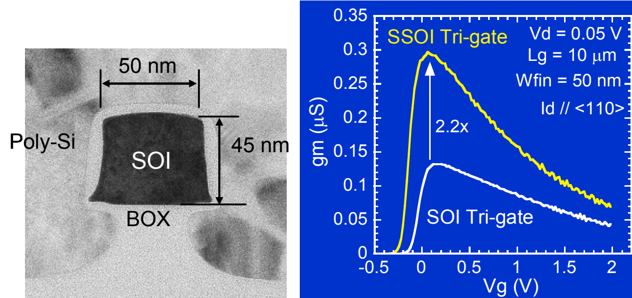


Fig. 4 S TEM photograph of fabricated Tri-Gate n-MOSFETs and Gm of the uniaxial strain and unstrained Tri-gate MOSFETs

We have confirmed that the electron mobility along <110> on (110) is significantly improved by tri-gate MOSFETs with uniaxial strain along <110> [22]. Fig. 6 also shows a TEM photograph of the cross section of fabricated Tri-gate n-MOSFETs using this uniaxial tensile strain channel, which can be created by the lateral strain relaxation for narrow Fins fabricated on biaxial SSOI substrates. The experimental G_m is compared between uniaxially strained and unstrained Tri-gate nMOSFETs with W_{fin} of 50 nm. As a result, a large value of the G_m enhancement of 2.2 is achieved, indicating that the fabricated device structure and the strain configuration can successfully increase the current drive of the multi-gate MOSFETs. Furthermore, as shown in Fig. 4, we have also found that the G_m value in the <110>-direction device with (110) sidewalls is 30% larger than that of the <100>-direction device with (100) sidewall, attributable to the electron repopulation into the 2-fold valleys as well as the effective mass reduction along <110> due to the uinaxial tensile strain along <110> [22]. These results have validated that <110> current flow and <110> uniaxial tensile strain is the best configuration for strained-SOI multi-gate structures.

Actually, this effective mass modulation in electrons due to <110> uniaxial tensile strain is caused by the effects of shear stress on the Si conduction band. Furthermore, this effective mass reduction can successfully be combined with the biaxial strain [23]. It is found in Fig.6 that (i) π_{shear} is constant whatever the initial biaxial stress in s-Si/$Si_{1-x}Ge_x$ devices whereas (ii) π_{biax} vanishes for x>20%. We thus conclude that (i) the shear stress impact on µe is fully additive with the initial global biaxial strain and (ii) only shear stress is responsible for the μ_e gain under <110> stress for s-Si/$Si_{0.7}Ge_{0.3}$, where all electrons occupy only 2-fold valleys in s-Si/$Si_{0.7}Ge_{0.3}$ and, thus, the further valley splitting should not have any influence on the µe gain. This is a direct evidence that the 2-fold valley warping under shear stress and the resulting effective mass reduction along <110> enhance μ_e, in agreement with [24].

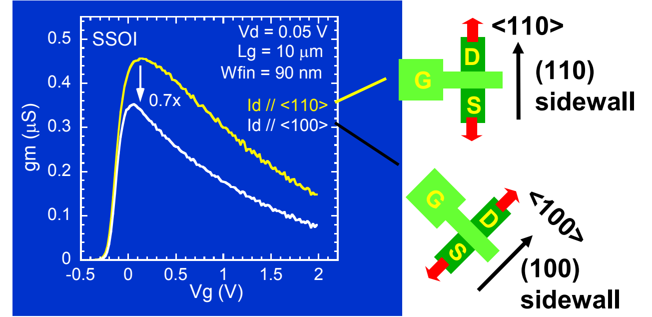
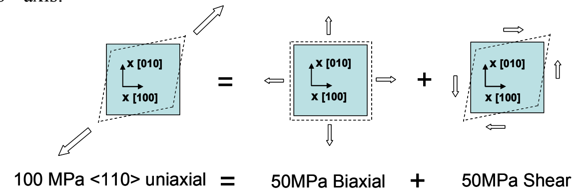


Fig. 5 Comparison in Gm between tri-gate n-MOSFETs along <110> and <100> axis.



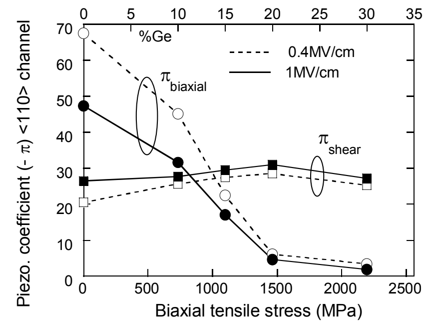


Fig. 6 Biaxial and shear piezoresistance coefficients extracted by longitudinal and transverse <110> stress for s-Si/SiGe devices with various %Ge (i.e.various initial biaxial tensile stress)

IV. Ge/III-V MOS Technologies

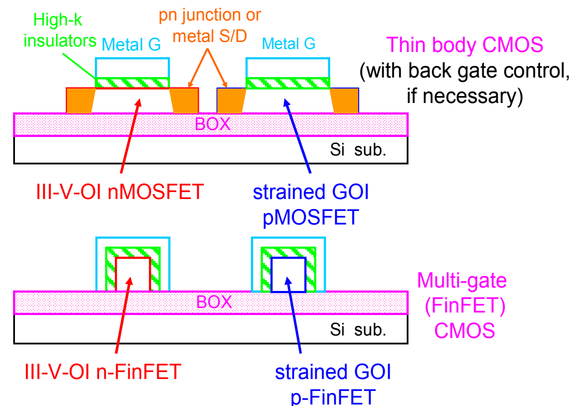


Fig. 7 Ultimate CMOS structure composed of the combination of III-V semiconductors n-MOSFETs and Ge p-MOSFETs on insulators

Ge/III-V semiconductors are expected to provide higher hole and electron current than the Si channels. We have proposed a typical CMOS using these channel materials with ultrathin body structures [25, 26], shown in Fig. 7. On the other hand, Ge and III/V MOSFETs share similar critical issues such as (1) gate insulator formation for superior MOS/MIS interface properties (2) high quality Ge/III-V channel formation on Si (3) improvement of carrier transport properties under inversion mode (4) S/D formation technology with low resistance/ leakage current (5) CMOS process integration technologies and demonstration of superior performance with short gate lengths.

Recently, there are recently many reports on superior interface control layers for Ge and III-V semiconductors, suggesting that appropriate gate stacks allowing us to provide high channel mobility will be available for these materials. Here, the reduction in the interface charges can be crucial in improving the channel mobility, as typically seen in Ge p-MOSFETs with Si passivation [27].

However, an essential problem in channel materials with the low effective mass such as III-V semiconductors is the low C_{inv} and resulting increase in the gate capacitance [11], while it can provide the high velocity. Fig. 8 shows the calculated I_{on}-V_g characteristics under full ballistic transport with gate oxide physical thickness (T_{ox}) of 3 and 0.5 nm [2, 28]. It is confirmed that the III-V channels become less effective in the I_{on} increase with decreasing T_{ox}. Thus, higher performance can be expected in III-V MOSFETs with thicker T_{ox}. While further optimization of III-V channel structures is still needed, these results suggest that there exists an optimized channel material, depending on T_{ox}.

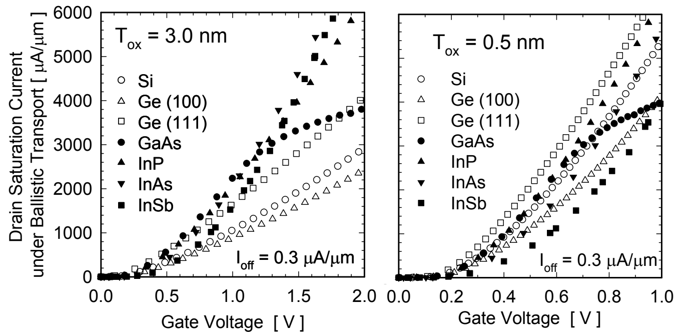


Fig. 8 Calculated I_{on} under full ballistic transport versus V_g with physical gate oxide thickness of 3.0 and 0.5 nm

V. Conclusions

For continuous and successive enhancement of CMOS performance, optimization of strain, surface orientation and channel materials including Si with optimized strain configuration, SiGe, Ge and III-V materials will be pursued through local and global process/device engineering and its combination. The comprehensive understanding of carrier transport properties in these new channels and any quantitative predictions for the device performance are mandatory in realizing these MOSFETs with minimal trials and errors.

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