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Strained Contact Etch Stop Layer Integration: Geometry Design Impact

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Abstract

Process induced stress is one of the key performance boosters to qualify advanced MOSFET technological node. 3D Finite Element simulation (FEM) is carried out to accurately model Contact Etch-Stop Layer (CESL) stress-related layout effects. Indeed, the corresponding stress field in transistors greatly depends on many parameters. Correlations with electrical measurements demonstrate results relevance. In addition to the effect of the transistor size, the environmental features of the MOSFET, such as the density of adjacent structures including dummy and Al-contact play a major role. As a result, differences in layout lead to considerably change the stress-induced transistor performance.

1 Introduction

Actual high density layout device featuring aggressive design rules with high Al-contact density, low poly-poly spacing and high dummy density, leads to significantly different CESL mechanical coupling compare to the ideal case describing an isolated device. If not properly predicted, such a variation can induce inaccuracies in SPICE transistor models depending on the specific design implementation.

In this work, the first challenge is to ensure an accurate prediction and a good understanding of CESL stress transmission by using Finite Element Method (FEM) involving mechanical and device simulations workflow. Layout dependence effect on CESL mechanical coupling is then discussed.

2 Modeling Strategy

Mechanical FEM using ANSYS© software was used to determine Si-channel average stress after mechanical equilibrium, assuming an elastic stress relaxation of strained nitride layer. The CESL has been investigated as a separated effect on transistor, surrounded or not by 2 poly-gate dummies thank to a 3D model, parameterized according to gate and active dimensions, dummy integration (poly-poly spacing and

dummy density), contact number and CESL properties (Figure 1). Periodic boundary conditions are used to emulate high density layout device.

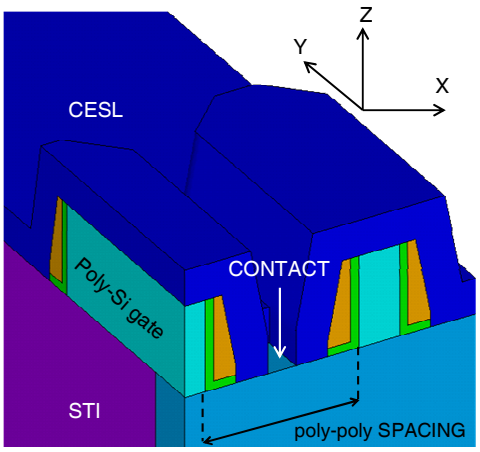

Figure 1: 3D quarter solid view of CESL strained MOSFET.

The corresponding On state current enhancement ratio A (1) compared to a stress free reference is obtained thanks to the development of a complete TCAD methodology [1] combining mechanical and electrical Monte Carlo simulations.

$$A = \frac{I_{on,stressed}}{I_{on,no\ stressed}} - 1 \tag{1}$$

3 Results and Analysis

The On state current enhancement ratio induced by tensile CESL is plotted as a function of the gate length (Figure2 (i)). Despite a high longitudinal stress increase (Figure2 (ii)), small devices characterized by short effect channel show a reduced sensitivity due to the increase of non strain sensitive components such as contact resistance increase. It also highlights that the experimental curves are well reproduced by the modeling flow: the discrepancies are within the uncertainties on the intrinsic stress level and thickness of the CESL on a patterned wafer and on process simulations. The simplified constant strain fields approach also captures most of the experimental features but the accuracy is somewhat lower. Thus, this simulation chain can be regarded as a sound basis to analyze these experimental data and give insight on the scalability of the performance enhancement.

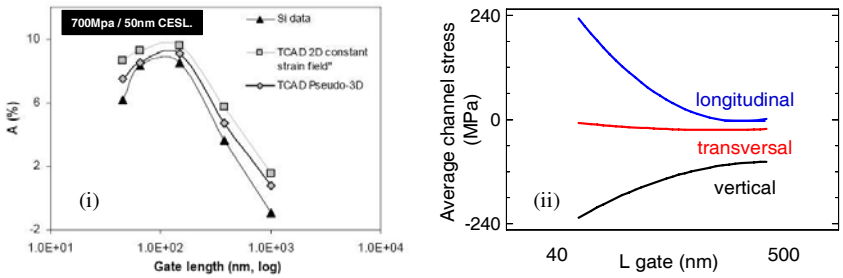

Figure 2: (i) Comparison of the current enhancement ratio as a function of the gate length with experimental data for a 50 nm thick – 750 MPa stressed CESL in the case of isolated MOSFET. (ii) Impact of gate length on average Si-channel stress. X-, Y- and Z-directions correspond to longitudinal, transversal and vertical direction respectively.

Simulation of both contact and dummy proximity effect leads to a decrease of modeled On state current enhancement ratio from roughly 14% to 8% compared to the virtual case of an isolated MOSFET with no contact and no dummy as shown in Figure 3. Indeed, contact and dummy proximity effect can be analyzed as a virtual removing of CESL capped on bulk-Si and STI (Shallow Trench Isolation) which reduces greatly the mechanical coupling as brought to the fore by the corresponding stress fields (Figure 4).

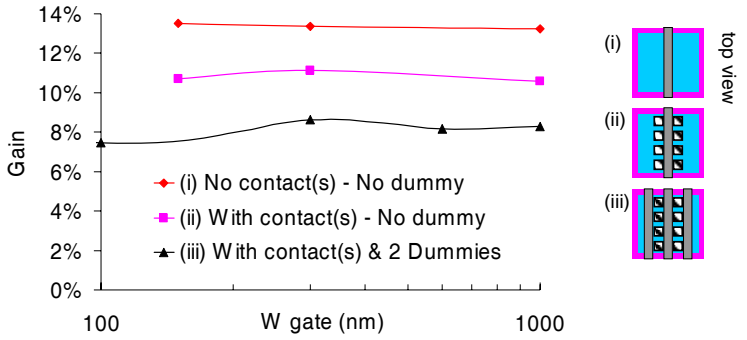

Figure 3: Impact of contact and dummy proximity on the current enhancement ratio induced by a +1.2 GPa CESL versus gate width (poly-poly spacing=0.205 µm, poly-to-STI=0.405 µm)

However both poly-poly spacing and density effect lead to such a performance decrease while poly-poly spacing effect remains limited in the case of low dummy density as shown in Figure 5. Basically, higher dummy density reduces the CESL capped on bulk-Si and STI which pulls Si-channel. More details and explanations on CESL stress transmission are given by Orain *et al.* [2].

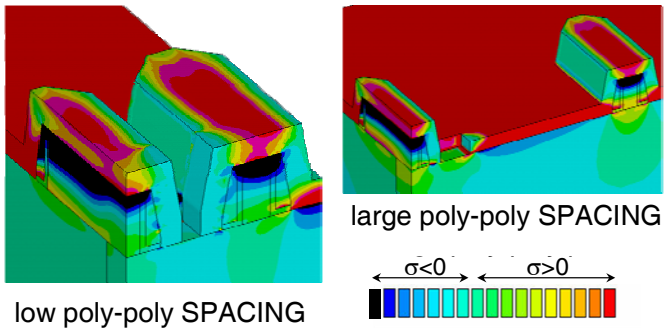

Figure 4: 3D longitudinal stress field view of CESL strained MOSFET for low and large poly-poly spacing.

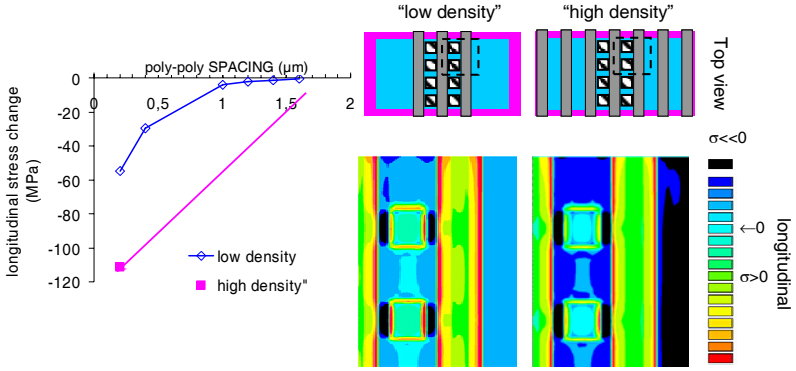

Figure 5: dummy density impact; (left) Si channel stress change versus low/high dummy density; (right) top quarter view of longitudinal stress field in Si-active versus dummy density (poly-poly spacing=0.205 µm, poly-to-STI=2.5 µm)

4 Conclusion

A wide range of issues related to the dependence of CESL efficiency versus layout is investigated through mechanical and device simulations. Detailed 3D simulations show how layout effects can impact the achievable transistor performance gain, SPICE models and circuit design. Indeed, the simulated electrical response varies dramatically from 0% up to 14% and higher with respect to geometrical parameters such as gate length, contact density, poly-poly spacing and dummy density.

References

[1] D. Villanueva *et al*., SISPAD Tech. Digest, pp. 320-321, 2005.
[2] S. Orain *et al*., "Method for managing the stress due to the capping layer", IEEE Trans. Elec. Dev., pp. 814-821.