Process Margin Analysis and Yield Enhancement Through Statistical Topography Simulation

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Abstract

One of the major challenges in deep submicron semiconductor era is to control the increase of variations due to decreasing in feature size. Currently, Design for Manufacturing (DFM) method enables to optimize layouts reducing the influence of process variations on circuit [1]. In this paper, we investigated the process margin analysis methods which are related to process defects of high aspect ratio (HAR) contact and short failures between lines. From this methodology, yield limiting process failures are identified and nano-scale defects in cells are virtually monitored without destructive method. This novel simulation methodology makes it possible to estimate the number of void defects of floating gate in Flash memory and predict Breakdown Voltage (BV) of the capacitor in DRAM. As a result, the defect level which is related yield has been decreased from 42% to 2.1% in 60nm Flash device and BV of capacitor has been virtually monitored in 80nm DRAM device.

1 Introduction

While device scaling meant the improvement of performance in the past, it doesn't just refer to performance improvement anymore nowadays. It means the increase of diverse variations besides the degradation of performance improvement [1]. For these reasons, from the viewpoint of design, the DFM tools are used to optimize layout and reduce variations [2]. However, regarding process variations, it is needed to consider process equipments and geometrical variations. We suggest the statistical simulation methodology for topography analysis which includes process variation both plasma processing equipments and geometrical parameters of device structure.

2 Statistical Simulation Methodology

Plasma is the key characteristic of deposition and etching in manufacturing process. Therefore, in order to account process variations, plasma processing equipments and geometrical parameters of device structure are considered. The plasma characteristic variations due to RF power and pressure such as ion and radical flux of plasma process equipment is simulated using CFD-ACE+. [3] The variations of process geometrical parameters like critical dimension of lines and thickness of thin film are used to get device structure. The PIE profile simulator which is the process integrated simulator using level-set algorithm provides the vertical device structure like Vertical SEM (VSEM) [4]. This profile simulator shows the detailed structure such as the void and the specific thickness of high aspect ratio (HAR) contact without conventional destructive method.

In some cases, thin film process results have a strong correlation between thickness and electrical characteristics. By continuous thickness and CD monitoring of in-fab data, fine fluctuations make statistical data of defect level or electrical characteristics. Furthermore, we can use this simulation methodology for prediction and optimization about process condition changes. Fig.1 shows the methodology of statistical topography simulation.

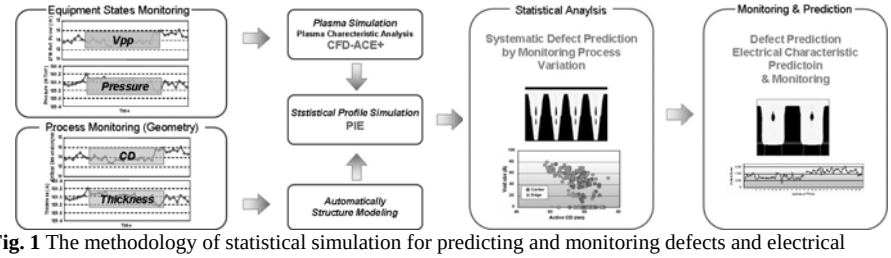


Fig. 1 The methodology of statistical simulation for predicting and monitoring defects and electrical characteristics. Fine fluctuations of equipments and process structure can effect to the final profiles.

3 Defect Margin Analysis

By using this simulation methodology, the 60nm NAND Flash cell has been analyzed to optimize a filling margin. Fig.2 shows the void problems which cause process failure such as bridge between floating gate lines and they also lead yield drop. During the process, there are various parameters which cause the defect profile. For example, RF source powers, pressure of plasma process equipments, various CDs and thickness of geometrical parameters. As the result of these parameters variations, the profile is also changes as shown in Fig. 3.

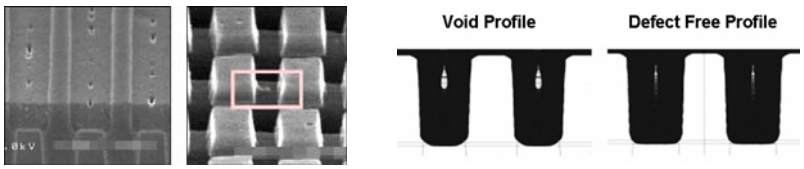


Fig. 2,3 The void defects in floating gate. Bridge caused by the void in flash cells. Simulated vertical profile differences, void profile and defect free profile by fluctuating critical parameters.

Sensitivity analysis is performed to find critical parameters. All available parameters are simulated by shifting mean value. And nitride and oxide thickness and active CD are chosen to critical parameters. Each parameter shows void size changes by shifting mean value of it as shown in Fig. 4. In order to optimize the defect free profile, statistical topography simulations are performed. The Monte-Carlo simulation results show that nitride thickness and active CDs contribute to void defects by 59% and 25%, respectively. Moreover, statistical Monte-Carlo simulation results can also show us the void-defect probability difference at the center and the edge of the wafer. In fig.5, the edge position of wafer is weaker than center about void defect.

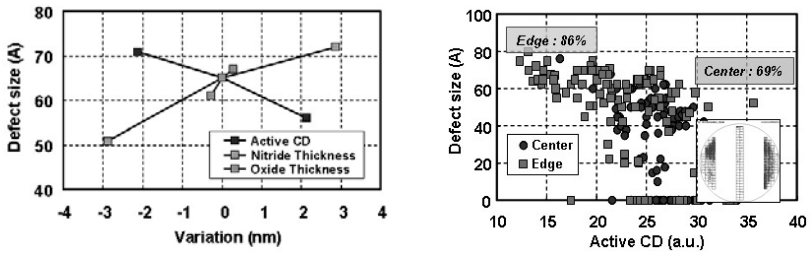


Fig. 4,5 The sensitivity analysis between defects size and critical parameters variations. Statistical result about void defects probability in a wafer center and edge.

Based on the results for the void probability in the wafer, the correlation between the probability and the real inspected void number in the wafer has been accomplished. It shows that we can predict the number of defects as the probability of them.

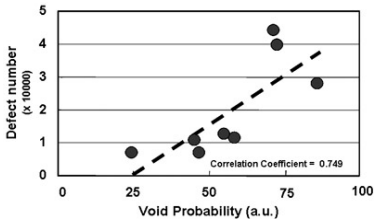


Fig. 6 The correlation between simulated void probability and real inspected defects number. It is well matched with 0.75 correlation coefficient.

We could reduce defect level from 42% to 2.1% in a wafer (Fig.7). Consequently, we contributed mass production condition to be stabilized in the early stage.

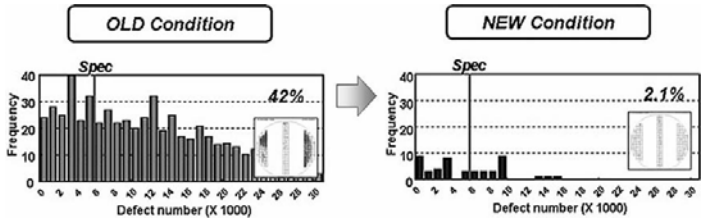


Fig. 7 The optimized result of defect-free condition. Spec-out wafer has been reduced from 42% to 2.1%

4 Breakdown Voltage Monitoring of Capacitor

Breakdown Voltage (BV) of DRAM cell capacitor is the minimum voltage that causes electrically current path in insulator. This weakened path makes leakage of cell capacitor and leads to failure of reading and writing data in DRAM cell. Therefore, BV is strongly related to the insulator thickness of cell capacitor. The Atomic Layer Deposition (ALD) is used for deposition of thin dielectric layer due to very good step coverage. However, HAR contact such as cell capacitor does not have good step coverage Fig. 8 shows HAR capacitor image in DRAM cell. In capacitor, bottom thickness of insulator is needed to optimize BV and secure cell leakage current. The insulator thickness is monitored at the large area pattern such as Open Site (OS) by ellipsometry as shown in Fig. 9. However, it is impossible to measure the bottom insulator thickness inside the pattern without destructive method.

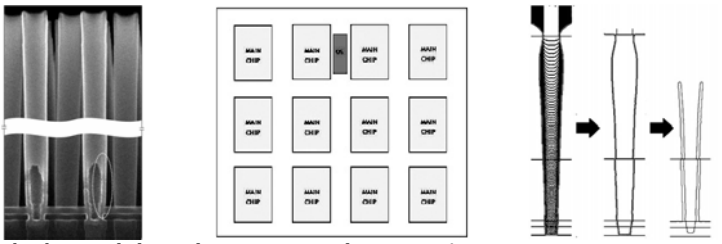


Fig. 8,9,10 Thin bottom dielectric layer causes BV drops in DRAM capacitor.
Thin film monitoring site is located separately at large area pattern.
Process integrated simulation in DRAM capacitor. It is simulated by using in–house tool, PIE.

Fig. 10 shows process integrated topography simulation and ALD modeling, bottom thickness of dielectric layer can be virtually monitored. In order to find out critical parameters which affect to capacitor bottom insulator thickness, sensitivity analysis is accomplished. Five critical parameters which affect on the bottom dielectric layer thickness are extracted as shown in Fig. 11.

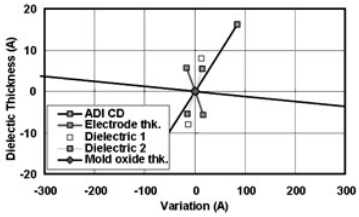
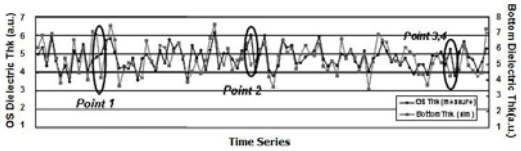


Fig. 11 Sensitivity analysis selects critical parameters. 5 critical parameters effect on bottom dielectric thickness are chosen.

Fig. 12 shows the measured thickness of OS site and bottom dielectric thickness by Monte-Carlo statistical topography simulation. Some points of simulation results are not well matched with monitoring thickness trends. For example, in 'Point 1' OS thickness increase but capacitor bottom thickness is decrease because mold oxide thickness and CD are increase. They make higher aspect ratio of capacitor than others and make it difficult to deposit in bottom. The other abnormal trends are analyzed in Table 1.



	Reasons
Point 1	Mold ox. ↑ CD ↓
Point 2	Mold ox. ↑ CD ↓
Point 3	Mold ox. ↑ CD ↓
Point 4	Mold ox. ↓ CD ↑ Electrode Thickness

Fig. 12, Table.1 The results of OS monitoring and bottom dielectric layer thickness in capacitor. Some points are not well monitored bottom dielectric thickness by OS site monitoring.
The analysis of the CD and thickness effect

Based on this simulation, the capacitor bottom dielectric thickness and the OS thickness are compared with BV. Fig. 13 shows that BV is more correlated with simulated bottom dielectric thickness than OS thickness. It means BV can be virtually monitored by dielectric thickness of capacitor bottom using profile simulation.

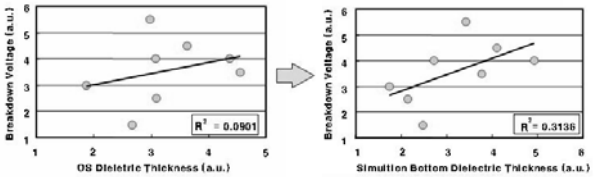


Fig. 13 BV has more correlation coefficient with simulated bottom dielectric thickness than OS monitoring data

5 Conclusion

We have developed the statistical simulation methodology for process margin analysis and virtual monitoring. By this novel methodology, we accomplished defect level reduction and electrical characteristic prediction in Flash and DRAM cell. The statistical topography simulation is needed to analyze defect with non-destructive method and enhance yield.

References

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[3] CFD-ACE+ online manual (http://www.esi-cfd.com/)
[4] W.Y. Chung et al., SISPAD 2000, pp. 127-130