Modeling and Extraction of Effective Lateral Doping Profile Using the Relation of On-Resistance vs. Overlap Capacitance in (100) and (110)-Oriented MOSFETs

Seong-Dong Kim*, Bin (Frank) Yang°, Shreesh Narasimha*, Andrew Waite°,
Karen Nummy*, Linda Black°, Haizhou Yin*, and Scott Luning°

*IBM Semiconductor R&D Center, Hopewell Junction, NY 12533, USA
{sdkim|snaras|knummy|yinh}@us.ibm.com

°Advanced Micro Devices, Hopewell Junction, NY 12533, USA
{fyang|awaite|blacklin|lunings}@us.ibm.com

Abstract

A comprehensive technique for the accurate extraction of the effective lateral doping abruptness and the spreading resistance components is applied to both Si (100) and Si (110) MOSFETs. The spreading resistance components under extension-to-gate overlap and spacer regions are successfully correlated to the lateral extension (EXT) doping abruptness by the relationship between on-resistance (R_{on}) and overlap capacitance response (C_{ov}). The lateral doping profile difference is extracted between (100) and (110) PMOS, which successfully explains higher external resistance in measured (110) PMOS.

1 Introduction

In short-channel MOSFETs, it has been reported that an optimal extension lateral doping profile could improve source/drain external series resistance (R_{ext}) as well as device short channel performance [1,2]. However, to date, the exact lateral EXT doping profile is still difficult to determine because neither a direct measurement method nor a comprehensive extraction technique is well established even with two dimensional (2-D) dopant profiling method such as scanning capacitance microscopy (SCM) [3]. Meanwhile, one of the novel approaches to extend the Si CMOS roadmap is hybrid-orientation technology (HOT) which builds NFET on (100)-Si-surface and PFET on (110)-Si-surface on the same wafer to improve carrier mobility through wafer and channel orientation engineering [4].
In this paper, a comprehensive method determining the effective lateral EXT doping abruptness and its correlation to the spreading resistance components are presented and applied to both Si (100) and Si (110) MOSFETs. This method successfully explains the R_{ext} difference between (110) and (100) PFETs.

2 Extraction Method

The physics-based R_{ext} components and the Gaussian function-based effective lateral doping abruptness are illustrated in Fig. 1 and in Ref. [5]. Physical modeling has shown that the R_{on} vs. C_{ov} contour is strongly dependent on the lateral doping gradient

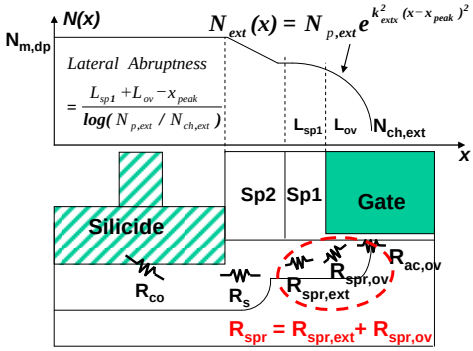


Figure 1: Schematic illustration of physics-based R_{ext} components. Total spreading resistance (R_{spr}) comprises spreading under offset spacer, Sp1 ($R_{spr,ext}$) and in gate overlap ($R_{spr,ov}$) and is found to be a strong function of EXT lateral abruptness.

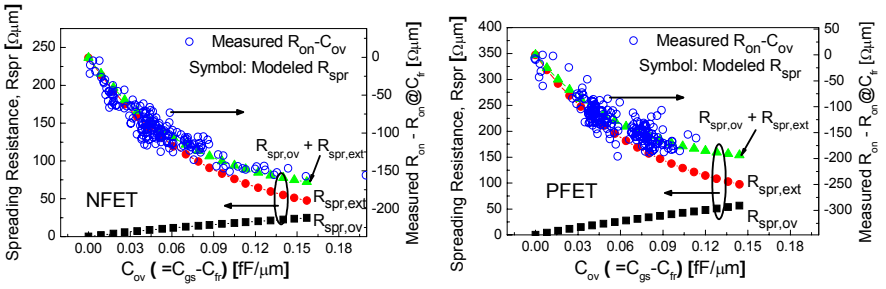


Figure 2: Model calibration/extraction of lateral doping abruptness and spreading resistance components using R_{on} vs. C_{ov} for (100) (a) NFET and (b) PFET.

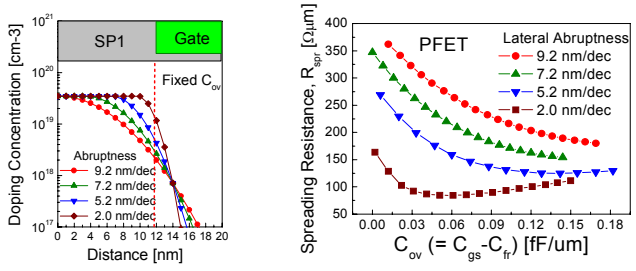


Figure 3: (a) Modeled lateral EXT doping profiles for different abruptness and (b) R_{spr} -C_{ov} responses in PFET at fixed $N_{ch,ext}$ and C_{ov}. Note that there is a substantial reduction in the spreading resistance component as profiles become highly abrupt box-like.

which determines the spreading resistance components under spacer 1 and EXT-to-gate overlap region. The effective lateral doping profiles of both NFETs and PFETs are extracted by calibrating physical spreading resistance model to R_{on} vs. C_{ov} response (at fixed L_{eff}) using typical characterization such as cross-section and 1-D SIMS analysis from 90nm-node SOI MOSFETs as shown in Fig. 2 [5]. The prediction

of R_{ext} vs. C_{ov} response for different extension lateral abruptness emphasizes the significance of EXT profile engineering towards highly steep box-like lateral profile in Fig. 3.

3 Lateral Abruptness of (100) vs. (110) PMOS

Fig. 4 shows relative R_{on}-L_{eff} characteristics for both (100) and (110) PMOS fabricated by the same 65nm-node baseline process. The (110) PMOS devices show higher R_{ext} which strongly depends on C_{ov}. The higher R_{ext} countervails the advantage of the higher (110) surface hole mobility [4]. I_{off}-I_{on} and I_{on}-C_{ov} characteristics in Fig. 5, respectively show noticeably large I_{on} sensitivity to C_{ov} in (110) PMOS as compared to (100) PMOS, consistent with the higher R_{ext} sensitivity to C_{ov} for (110) devices shown in Fig. 4. It should be noted from the experimental R_{on} vs. C_{ov} curves in Fig. 6(a) that (110) PMOS shows apparently higher slope (i.e., $\Delta R_{on}/\Delta C_{ov}$) than (100) PMOS. Applying our extraction method, the modeled R_{on}-C_{ov} responses of both (100) and (110) PFET can be fit reasonably well with those of experiment after calibration of the lateral EXT doping parameters in Fig 6(a). The extracted lateral EXT doping parameters are used in spreading resistance calculation for both (100) and (110) pMOS and finally higher levels of spreading resistance component are resulted in (110) PMOS due to the lower tail doping profile, as shown in Fig. 6(b) which explains higher R_{ext} and hence R_{on} in (110) PMOS than (100) PMOS.

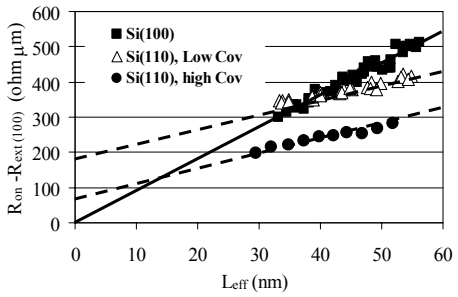
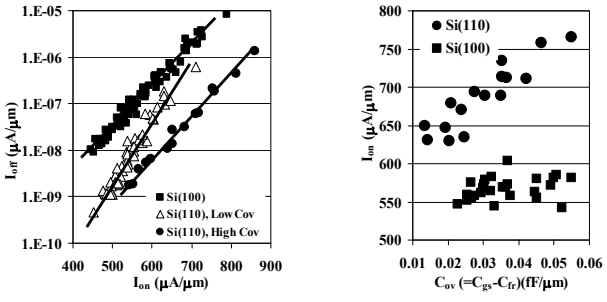
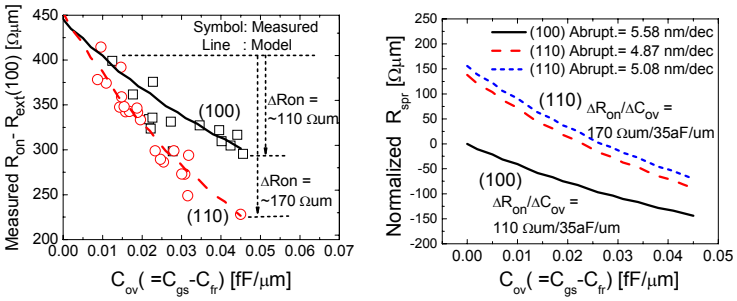


Figure 4: Relative R_{on}-L_{eff} plots for both (100) and (110) PMOS. All R_{on} values were subtracted by the R_{ext} of the (100) PMOS.



(a) (b)

Figure 5: (a) I_{off}-I_{on}, and (b) I_{on}-C_{ov} at I_{off}=1E-7μA/μm plots for both (100) and (110) PMOS. Note, I_{on} keeps increasing with C_{ov} for (110) but not for (100), consistent with Fig.4 where R_{ext} for (110) decreases with increasing C_{ov}.



(a) (b)

Figure 6: (a) Lateral abruptness calibration to measured R_{on} vs. C_{ov} of (100) and (110) PMOS and (b) resultant normalized relative spreading resistance with C_{ov} after calibration.

4 Conclusion

A comprehensive method to determine the lateral doping abruptness and spreading resistance component is presented in this paper. By applying this method to analyze R_{ext}, it is found that there is a lateral doping profile difference between (100) and (110) PMOS, which explains why the (110) PMOS R_{ext} is higher than that of (100) PMOS.

Acknowledgements

This work was performed by the Research Alliance Teams at various IBM Research and Development Facilities.

References

[1] Y. Taur, C.H. Wann, and D.J. Frank, "25nm CMOS design considerations," in *IEDM Tech. Dig.*, pp. 789-92, 1998.

[2] M.Y. Kwong, R. Kasnavi, P. Griffin, J.D. Plummer, R.W. Dutton, "Impact of lateral source/drain abruptness on device performance," *IEEE Trans. Electron Devices*, vol. ED-49, pp. 1882-1890, 2002.

[3] A.C. Diebold, M.R. Kump,J.J. Kopanski, and D.G. Seiler, "Characterization of two-dimensional dopant profiles: Status and review," *J. Vac. Sci. technol. B, Microelectron. Process. Phenom.*, vol. 14, pp. 196-201, 1996.

[4] M. Yang , M. Ieong, L. Shi, K. Chan, V. Chan, A. Chou, E. Gusev, K. Jenkins, D. Boyd, Y. Ninomiya, D. Pendleton, Y. Surpris, D. Heenan, J. Ott, K. Guarini, C. D'Emic, M. Cobb, P. Mooney, B. To, N. Rovedo, J. Benedict, R. Mo, and H. Ng, *et al*, "High performance CMOS fabricated on hybrid substrate with different crystal orientations," in *IEDM Tech. Dig.*, pp. 453-456, 2003.

[5] S.-D. Kim, S. Narasimha, and K. Rim, "An integrated methodology for accurate extraction of S/D series resistance components in nanoscale MOSFETs," in *IEDM Tech. Dig.*, pp. 155-158, 2005.