Device Design Evaluation of Multigate FETs Using Full 3D Process and Device TCAD Simulation

Muhammad Nawaz, Stefan Decker, Luis-Felipe Giles, Wolfgang Molzer, Thomas Schulz, Klaus Schrüfer and Reinhard Mahnkopf

Infineon Technologies AG, Am Campeon 1-12, D-81726 Munich, Germany
Muhammad.Nawaz@infineon.com

Abstract

Full 3D numerical process and device simulations have been performed in order to optimize device design of multigate FETs (MuGFETs) and the underlying fabrication processes. At first process simulation parameters have been calibrated to measurement data of pre-development process results. Based on this, device electrical performance has been assessed for different gate length, fin doping, implant conditions, fin height, fin width, gate oxide and box thickness by means of typical device parameters.

1 Introduction

As the scaling of bulk MOS devices is reaching to its ultimate limit, double (FinFET) or triple (Tri-Gate) gate Multi-Gate FET (MuGFET) devices are emerging as strong candidates for low power or high performance applications in the future. This work reports on the theoretical design evaluation of MuGFETs using commercial three-dimensional (3D) TCAD simulation tool. All critical process steps (i.e., channel implant, gate oxide growth, extension implant, halo implant, spacer formation and source-drain implant) alongwith complete thermal budget for tri-gate MuGFETs on standard SOI have been included in the process simulation. The total number of mesh points for one half of the device was approximately 180,000, while the computation time was 10-12 hours. Device simulations have been performed using drift diffusion model taking into account quantum confinement effects, bandgap narrowing effects, low field (doping and temperature dependence) and high field mobility models including surface scattering model of Lombardi. A TiN metal gate with workfunction of 4.65 eV was used in the device simulation.

2 Results and Discussion

An internal view of simulated MuGFET structure and TEM image of a real fin is shown in fig. 1. Following the implementation of our realistic process flow, first the junction position was calibrated. Using the default model of transient activation of dopants in Si with an activation time of $8 \cdot 10^{-16}$ s, the lateral diffusion of As in Si is highly unrealistic, as it induces 14 nm gate overlap region on each side of the gate with a correspondingly overestimated overlap capacitance. On the other hand, using a too long activation time, the on-current decreases because of a too low active As concentration of $2 \cdot 10^{19}$ cm^{-3} in the source/drain area which leads to a too high sheet resistance. A reasonable choice for the activation time suggests $8 \cdot 10^{-15}$ s which results

in a vertical junction profile along the fin height with a reasonable gate overlap of 8 nm on each side of the gate and an active As concentration of $0.9–1.0{\cdot}10^{20}$ cm^{-3}, see fig. 2. Using realistic process flow, our 3D process and device simulation results were calibrated with experimental data and fairly show good agreement (fig. 2: right). Hence this data provides a reliable base for studying further device scalability.

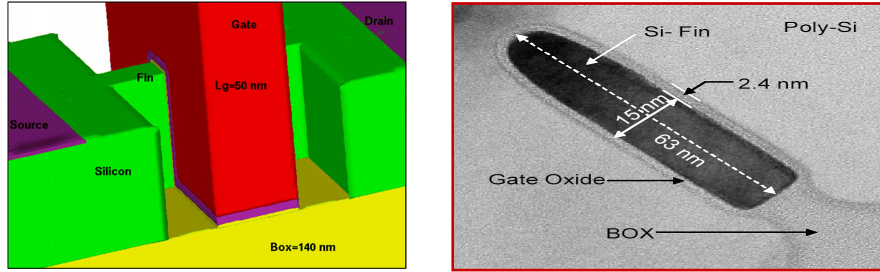

Figure 1: Internal view and TEM image of a real Fin with height of 63 nm, width of 15 nm and gate oxide of 2.4 nm.

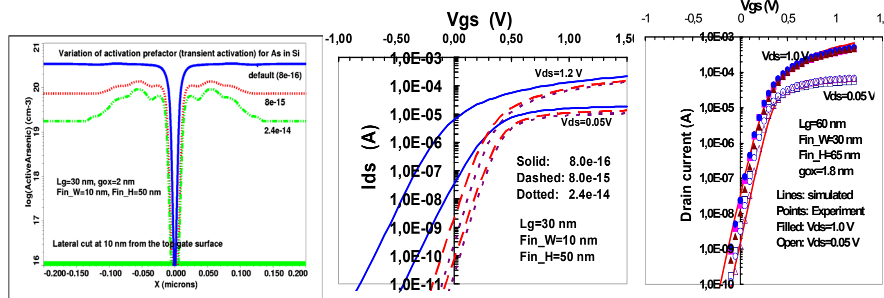

Figure 2: A lateral cut (left) and transfer characteristics (middle) with different transient activation time of As diffusion in Si and comparison with experimental data.

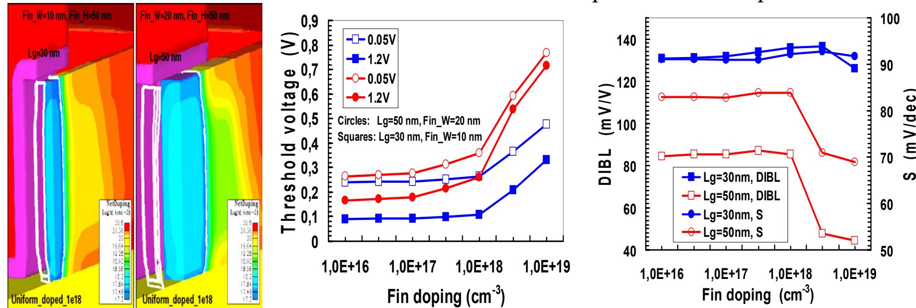

Figure 3: Net doping profile, threshold voltage, DIBL/S as a function of fin doping.

As long as the fin is fully depleted due to low or moderate uniform fin doping, the threshold voltage and short channel effects negligibly depend on the doping level for fin width Fin_W=10 nm at a gate length Lg=30 nm, and Fin_W=20 nm at Lg=50 nm, see fig. 3. Only with very high fin doping, the threshold voltage V_{th} increases and drain induced barrier lowering (DIBL) and subthreshold slop S drop along with a significant decrease in the on-current I_{ON}. At constant fin width, I_{ON} and transconductance G_m approximately increase linearly with increasing fin height. V_{th},

DIBL and S are approximately independent of fin height at fixed fin width, see fig. 4. On the other hand DIBL, S and off-current I_{OFF} are quite sensitive to variations in fin width. Fairly good agreement of S and DIBL values with experimental data (fig. 4: data of Lg=75 nm, Fin_W=25 nm, Fin_H=65 nm) from different devices further validates our simulation work. Although I_{OFF}, DIBL and S are smaller for thinner fin devices, the delay $\tau_d = C_{GG} \cdot V_{DD}/I_{ON}$ and intrinsic cutoff frequency $f_T = G_m/(2\pi C_{GS})$ improve with thicker fins (Fin_W=20 nm at Lg=30 and 50 nm), see fig. 4.

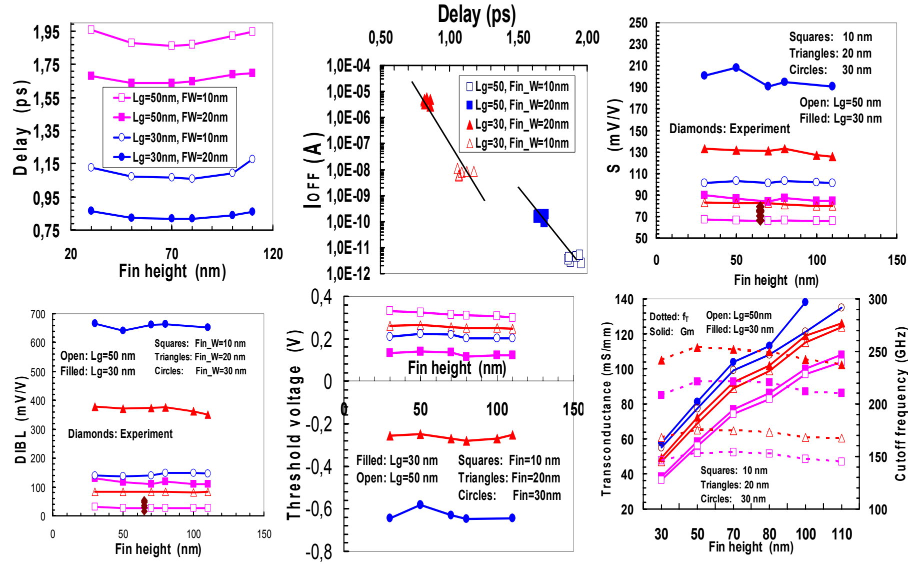

Figure 4: Delay, I_{OFF}, S, DIBL, V_{th}, G_m, and f_T plotted as a function of Fin height and for different Fin width.

In addition to the impact of fin geometry, the tilt angle of the As extension implant has been investigated. For a given fin height, the on-current increases by about 15–20% when increasing the tilt angle while I_{OFF} changes approximately one order of magnitude. A tilt angle of 10–60º induces variation in DIBL of 40–46% and S of 12–15%. Although, the on-current is higher for 45–60º, a tilt angle as low as 20–30º (in the real process it is 45º) is advantageous for controlling short channel effects (fig. 5) and leakage as can be seen by the current density in the off state (fig. 6 right). Moreover, it is critical to facilitate the processing of multiple and tall fin devices (i.e., large width devices). The delay and transconductance remain approximately unaffected with tilt variation from 20–60 degrees (fig. 5).

Compared to planar MOSFETs, MuGFETs show a relatively smaller body factor $\gamma = \Delta V_{th}/\Delta V_{SB}$, where a substrate bias V_{SB} of 0 V and -1.2 V was used. Due to geometrical effects, for a given box thickness, the body factor (fig. 6) is higher for longer gate and thicker fin devices. Similarly, I_{OFF} increases with decreasing box thickness. Extracted values of overlap (C_{OV}) and gate-bulk (C_{GB}) capacitances (fig. 6) show a variation of 8% and 78% respectively when decreasing the box thickness from 140 nm to 25 nm (fig. 6). With a fixed box thickness, C_{OV} is 5% higher for a fin width of 20 nm when compared to 10 nm (not shown). A reasonable good agreement of

extracted value of overlap (plus fringe) capacitance from real device further supports our simulation data (fig. 6).

Finally, investigation of gate oxide thickness shows that the DIBL and S reduce with thinner gate oxide. Note that the threshold voltage increases with the increase of gate oxide thickness for longer gate (i.e., 50 and 80 nm: L_g/L_{ov} is large) MuGFET, as expected. However, this trend shows an opposite behavior of V_{th} for smaller gate length (i.e., 30 nm: L_g/L_{ov} is small) due to increased gate overlap.

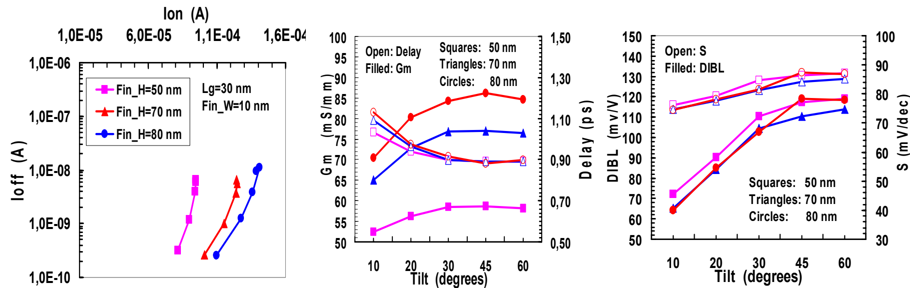

Figure 5: I_{OFF} /I_{ON} behavior, G_m and Delay, DIBL/S with varying Ldd implant tilt.

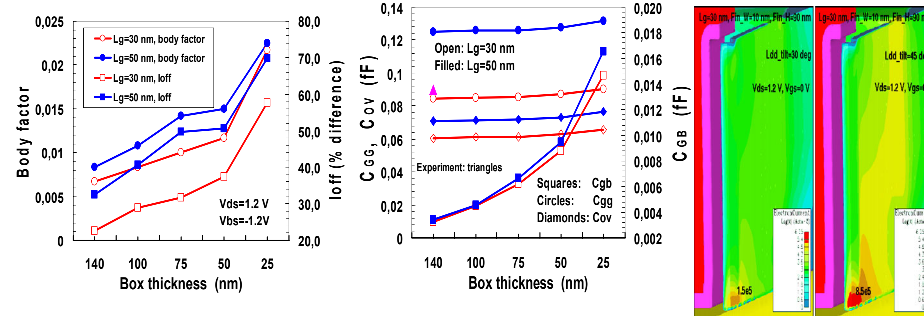

Figure 6: Body factor, I_{OFF} difference, and gate capacitances with variation of Box thickness. Experimental symbol (middle) for extracted overlap plus fringe capacitance with box thickness of 140 nm and Lg=75 nm. Current density for different Ldd tilt.

3 Conclusion

Using full 3D process and device simulation, our findings provide a useful guide for process and device optimization. Firstly, a low or moderate fin doping along with lower extension tilt angel is beneficial not only to reduce I_{OFF}, DIBL and S but also to facilitate processing of multiple and tall fin structures. Secondly, keeping device scalability in mind, new simulated device parameters like delay, f_T, capacitances, and body factor based on realistic process flow provide a useful guide to circuit designer for analog, RF and digital applications.

Acknowledgements

This research is supported by the European Commission's Information Society Technologies Programme under PULLNANO project contract No. IST-026828.