The Optimization of Low Power Operation SRAM Circuit for 32nm Node

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Abstract

As CMOS technology is advanced in recent years, the operation of SRAM becomes critical issue for further scaling. It is crucial for realizing the SRAM to keep static noise margin (SNM) and write margin (WM) large enough to get stability and overcome random dopant and process fluctuations. Also, suppression of leakage current is another key issue. The major sources of leakage current are the gate direct tunneling current, the sub-threshold leakage and the reverse biased band-to-band-tunneling junction leakage. To reduce total chip power, these leakage components must be suppressed.

In this paper, we have focused on the optimization of low power operation SRAM circuit for 32 nm node with TCAD optimizing the relationship among margin, leakage current and access time. To conduct the circuit design principle, we define the new quality factor and evaluate the 32nm SRAM performance with this defined formula.

1 32nm technology SRAM design

Firstly, we design the 32nm technology low operation power (LOP) transistor. The target is decided by ITRS 2006[1]. Design parameters and characteristics are shown in Table 1. In this calculation, we consider three leakage currents, which are gate direct tunneling, sub-threshold leakage and reverse biased junction leakage. For device design parameters, we mainly evaluate substrate dopant density, halo dopant density and extension depth (Fig. 1).

	NMOS	PMOS
L_{poly} (nm)	22	22
V_{dd} (V)	0.7	0.7
I_{on} (μA/μm)	700	350
I_{off} (μA/μm)	20	10

Table 1: Design parameters.

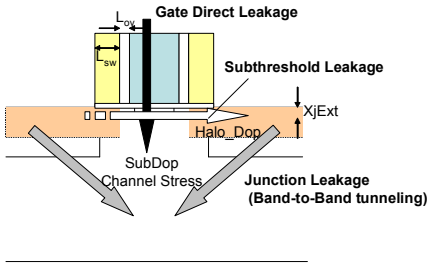

Figure 1: Design parameters and leakage components in a transistor.

We simulated sensitivity analysis for these three parameters and draw the design window as shown in Fig. 2. We show the final characteristics of NMOS and PMOS in

Fig. 3. Designed parameters are listed in this figure. Both characteristics meet the demands of roadmap.

Secondly, we show 6-transistor type (6T) SRAM cell and 8T SRAM cell circuit and dominant stand-by leakage path in Fig. 4. In this paper, we also consider wire capacitance. Bit line and word line capacitances directly influence SRAM access time. These values are directly calculated by means of 3-dimensional interconnect simulator Raphael [3] by which we can include device geometrical effect from mask layout. In Fig. 5, the parasitic capacitances of Bit line and Word line are evaluated for 6T and 8T and some cell ratios (β ratio). β ratio is defined by the ratio of the pull down (driver) to pass gate (transfer) transistor.

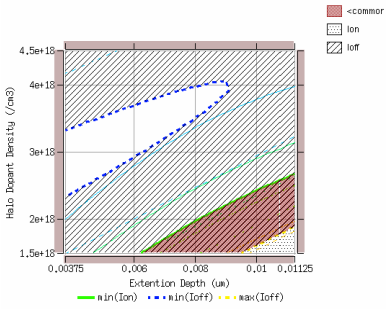

Figure 2: Design window for extension depth and halo dopant density.

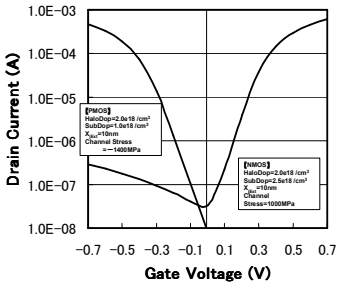

Figure 3: Optimized device characteristics for 32nm

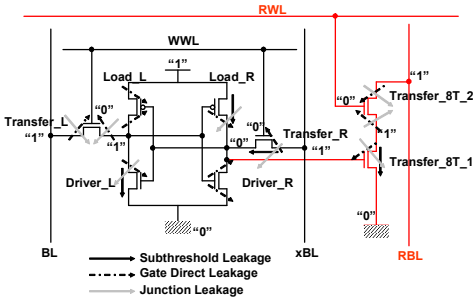

Figure 4: 6T and 8T SRAM circuit and dominant leakage path in stand-by mode.

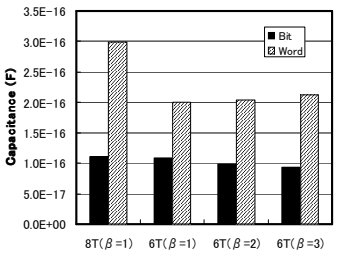

Figure 5: Extracted capacitances by 3D simulation.

2 Introduction of Quality Factor and Evaluation

Although SRAM quality factor concerning with access time and leakage current is defined in [2], this is not enough for circuit stability evaluation. In this paper, we propose new quality factor of SRAM as follows:

$$QF = \frac{(SNM \cdot WM)^C}{T_{access}^A \cdot I_{leak}^B} \tag{1}$$

In this paper, we define A=1, B=1, C=0.5 for simplicity. This equation can be divided into three parts and interrupted as followed meaning.

$$QF = \frac{\sqrt{SNM \cdot WM}}{T_{access} \cdot I_{leak}} = \frac{1}{C} \cdot \frac{\sqrt{SNM \cdot WM}}{V_{dd}} \cdot \frac{I_{read}}{I_{leak}} \quad (2)$$

First term is parasitic capacitance part, and second is standardized operating margin part, and final is switching capability part.

Before analyzing this proposed quality factor, we calculated the margin as functions of β ratio and pull up ratio (PUR). Pull up ratio is defined by the ratio of the pull up (load) to pass gate (transfer) transistor. Fig. 6 shows the relation between margin and β and pull up ratios. SNM increases as both β ratio and PUR increase. WM increases as both β ratio and PUR decrease. From this result, it is clear that SNM and WM have the trade-off relationship. Therefore, we should search the optimum design point.

Next, we will evaluate several proposed improving design techniques. We compared some 6T SRAMs (referenced, $V_{cell}=V_{dd}+0.2V$, β =3.0, PUR=0.5) and 8T SRAM. In Fig. 7, Quality factor is plotted as a function of channel dopant density in NMOS transistor. 8T SRAM exhibits the best performance, but area becomes 40% larger than conventional 6T SRAM. To operate SRAM circuit with stability, both SNM and WM should be kept large enough as well as circuit quality factor. Both quality factor and WM increase as PUR decrease. While SNM increase as β ratio increase, quality factor decreases. We investigated this trade-off relationship for β ratio in details.

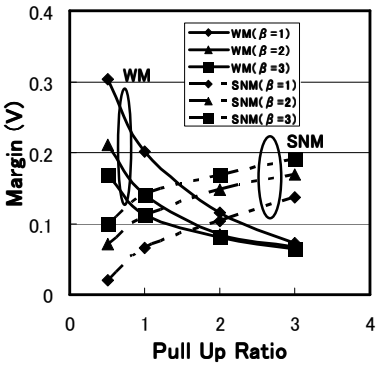

Figure 6: Margin and cell ratio

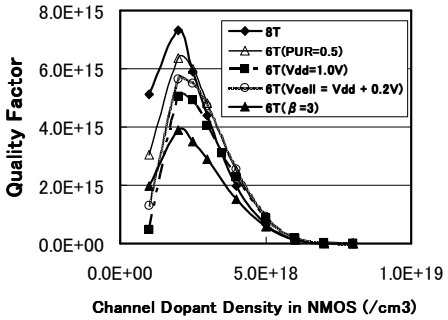

Figure 7: Quality factor in NMOS

In Fig. 8, we show the quality factor and effective margin (EM), $\sqrt{SNM \cdot WM}$, as functions of β ratio and PUR. EM increases as β ratio increases and PUR decreases. But quality factor decreases as β ratio increases. To clarify this trade-off relationship, total leakage current of SRAM circuit as a function of ratio is shown in Fig. 9. For PUR, total leakage current little depends on cell ratio. On the other hand, total leakage current increases dramatically with β ratio increase. From this result, quality factor decreases because leakage current increases dramatically instead of the improvement of SNM. In addition, we investigated leakage components more precisely for each transistor. Fig. 10 describes the leakage current for each transistor. Leakage current of driver_R and transfer_L are dominant factors. As shown in Fig. 4, the main source of this leakage current is the gate direct tunneling current. To achieve the improvement

for both quality factor and SNM, we should reduce the gate leakage current of these transistors. As already known well, high-k materials for gate insulator are very effective to decrease leakage current. Then, we show the quality factor for both k=3.9 and 5.0. By using the gate insulator material which dielectric constant is 5.0, we can get high performance condition (β=2, PUR=0.5). This condition exceeds 8T SRAM performance and the area of total circuit is also less than 8T SRAM type.

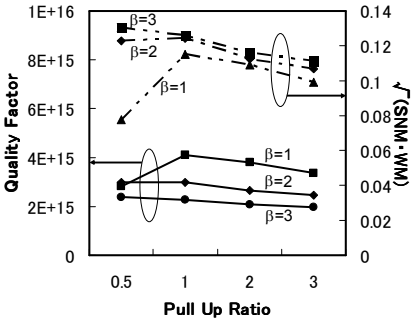

Figure 8: Quality factor and effective margin

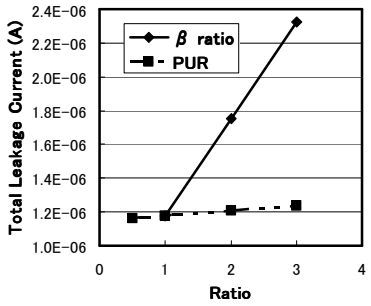

Figure 9: Leakage current and Ratio

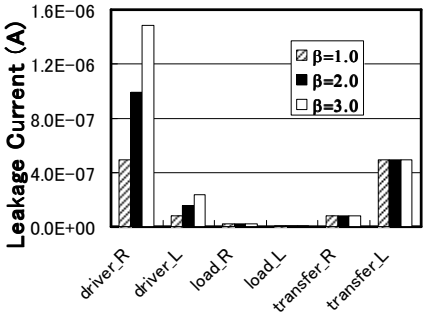

Figure 10: Leakage current in each transistor

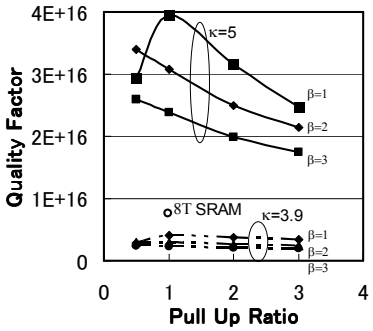

Figure 11: Quality factor for high-k

3 Conclusion

We have focused on the optimization of low power operation SRAM circuit for 32 nm node with TCAD technique by accounting for margin, leakage current and access time. From these considerations, we can conclude that the suppression of leakage current is very critical issue to achieve both high total circuit quality and stability.

References

[1] http://public.itrs.net/
[2] "Circuit-aware Device Design Methodology for Nanometer Technologies: A Case Study for Low Power SRAM Design," Design, Automation and Test in Europe, Vol. 1, pp. 1- 6, 2006.
[3] Raphael manual, Synopsys Inc.