# Process Variation-Aware Estimation of Static Leakage Power in Nano CMOS

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**Abstract**

We present a statistical methodology for leakage power estimation, due to subthreshold and gate tunneling leakage, in the presence of process variations, for 65 nm CMOS. The circuit leakage power variations is analyzed by Monte Carlo (MC) simulations, by characterizing NAND gate library. A statistical "hybrid model" is proposed, to extend this methodology to a generic library. We demonstrate that hybrid model based statistical design results in up to 95% improvement in the prediction of worst to best corner leakage spread, with an error of less than 0.5%, with respect to worst case design.

## 1 Introduction

Process variability and its impact on circuit design is critical to power management in sub-90 nm CMOS designs. Leakage constitutes about 33% of the total circuit power and it increases with technology scaling. Moreover, increasing process variations result in significant increase in leakage power and its spread. Variations in chip level leakage current of 20X is observed. Traditional circuit design techniques based on worst case leakage result in extremely pessimistic designs with lower performance. Hence, there is a need for variation-aware, reliable and accurate estimation of leakage power.

Several methods have been proposed for predicting leakage power and its variations. The subthreshold and gate leakage power of a circuit is analyzed considering spatial correlations due to intra-chip variations [1]. Leakage power and its variability can be reduced significantly by biasing the gate length of transistors not in the critical paths, for a small delay penalty [2]. In this direction, we present a statistical methodology to estimate the leakage power by directly relating to underlying process parameters. A Technology Computer-Aided Design (TCAD) tool [3] for process simulations and a general purpose circuit simulator SEQUEL [4] for circuit simulations, are used.

## 2 Characterization of leakage power of NAND gate

The simulation flow, that transforms the process variations to relevant leakage power distributions, is illustrated in Fig. 1. The 65 nm gate length NMOS/PMOS devices are designed and optimized, for a leakage of 10 $nA/\mu$m at $V_{dd}$=1.2 V, by process simulations. A set of significant process parameters, gate length ($L_g$), gate oxide thickness ($T_{ox}$), halo dose, Super Steep Retrograde Channel (SSRC) dose, halo tilt angle and anneal temperature, is identified and their variations are assumed to have a Gaussian distribution with a $\pm 3\sigma$ variation of $\pm$10% [5]. A set of NMOS/PMOS devices with variations in each of the 6 process parameters are generated. The simulator is calibrated to provide experimentally measured values of gate direct tunneling current density of

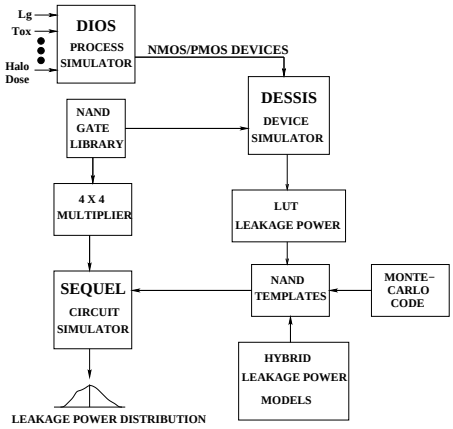


**Figure 1:** Block diagram of simulation flow.

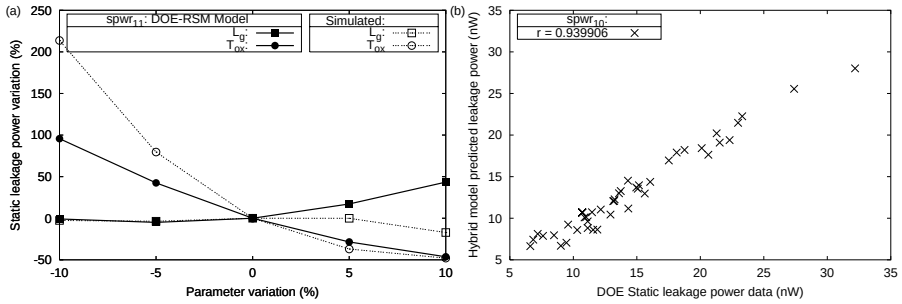


**Figure 2:** (a) Simulated and DOE-RSM modeled leakage power variations with process variations. (b) Correlation plot of hybrid model predicted leakage power Vs. DOE data.

10 $A/cm^2$ for NMOS and 1 $A/cm^2$ for PMOS. Using these devices, a single-stage 2-input NAND gate is mixed-mode simulated to obtain total leakage power for all input combinations ($spwr_{00}$, $spwr_{01}$, etc.), and their respective look-up tables are generated.

## 3 Modeling Methodology

To model the impact of multiple process variations on leakage power, Design of Experiments (DOE) is performed and second order models are built using Response Surface Methodology (RSM) [6]. A 3-level Face Centered Central Composite (FCCC) design for 6 process parameters is performed with 52 experiments, out of a large set of $3^6$ full factorial design. Models obtained, using simulation data, are polynomials of the form

$$y = \beta_0 + \beta_1 x_1 + ... + \beta_6 x_6 + \beta_{12} x_1 x_2 + ... + \beta_{56} x_5 x_6 + \beta_{11} x_1^2 + ... + \beta_{66} x_6^2 \qquad (1)$$

where $\beta_0$ is the nominal response, $x_i$s are normalized process parameters, and $\beta_i$s are regression coefficients obtained from response surface DOE data, for i = 1, ..., 6.
Fig. 2(a) shows variations in leakage power versus process, obtained by simulations and the DOE-RSM model. As 3-level FCCC design is inadequate to fit the response seen, a third order rotatable design with 240 experimental runs is needed, resulting in 5X rise in computations. To achieve this response fit with 3 levels, $-10\%$ to $+10\%$

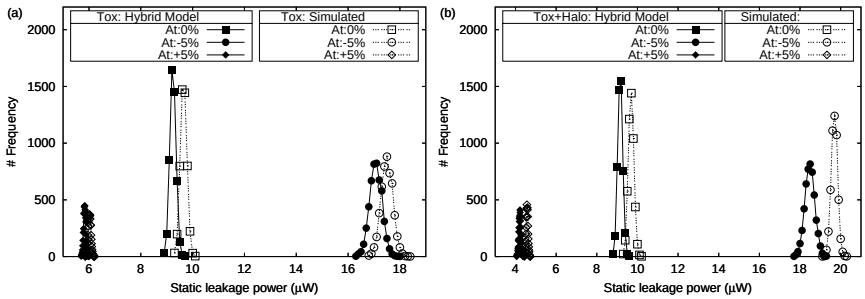


**Figure 3:** Simulated and hybrid modeled leakage power distribution for: (a) variations in $T_{ox}$ (b) simultaneous variatons in $T_{ox}$ and halo dose.

**Table 1:** Statistics of leakage power distribution for $T_{ox}$ and halo dose variatons(in $\mu W$).

| Statistics | Simulated | | | Hybrid Model | | |
|---|---|---|---|---|---|---|
| | At -5% | At 0% | At +5% | At -5% | At 0% | At +5% |
| Nominal power | 20.44 | 9.17 | 4.36 | 18.18 | 9.17 | 4.15 |
| Distribution mean | 19.69 | 9.68 | 4.56 | 18.48 | 9.15 | 4.26 |
| Median | 19.69 | 9.68 | 4.56 | 18.48 | 9.15 | 4.26 |
| Std. deviation | 0.2152 | 0.1316 | 0.0442 | 0.2395 | 0.1172 | 0.0513 |
| Best corner power | 9.17 | 4.36 | 3.75 | 9.17 | 4.15 | 3.50 |
| Worst corner power | 20.25 | 20.44 | 9.17 | 19.54 | 19.18 | 9.17 |

range is split into two regions: $-10\%$ to 0% and 0% to $+10\%$. A piece-wise quadratic model obtained as a function of every process parameter and in each of these regions is

$$y = \beta_0' + \beta_1' x_i + \beta_2' x_i^2 \tag{2}$$

where $\beta_i'$s are the regression coefficients determined using Least Squares Method (LSM). A second order "hybrid model" is generated, whose constant, linear and quadratic terms come from LSM model and correlation terms come from DOE-RSM model. Though the model is somewhat heuristic, this idea of fitting higher order response surfaces with piece-wise quadratic models, proves to be computationally efficient and yet very effective. Experimental and hybrid model predicted response correlate well with correlation coefficient in the range 0.88 to 0.94 (Fig. 2 (b)), and thus validating the hybrid model.

## 4 Leakage Power Distributions of A Digital Circuit

The steady state analysis of a 4-bit $\times$ 4-bit Wallace tree multiplier made of 2-input NAND gate library, is performed to obtain its leakage power, using SEQUEL. The systematic and random variations are appropriately modeled and leakage power distributions are obtained through MC simulations, using data from the mixed-mode generated look-up tables and the hybrid model. For $T_{ox}$ variations, hybrid model predicted distributions match well with those of mixed-mode simulations, as shown in Fig. 3(a).

To generalize the methodology for simultaneous variations in multiple processes, 2 significant process parameters, $T_{ox}$ and halo dose, from the perspective of variability, are taken. A look-up table of leakage power is generated, corresponding to 25 device/circuit splits with nominal, $\pm 5\%$ and $\pm 10\%$ variations in 2 parameters. The leakage power distributions are obtained by applying two-dimensional interpolation on look-up table and by hybrid model (Fig. 3(b), Table 1). The hybrid model predicted mean, standard deviation and corner powers are in error by less than 6.7%, 16%, 6.6%, respectively.

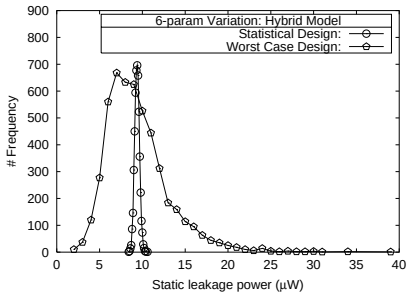


**Figure 4:** Leakage power distributions with statistical design and worst case design using Hybrid model for variations in 6-parameters, for $\pm 3\sigma = \pm 10\%$ at nominal.

**Table 2:** Statistics of leakage power distribution for variations in 6-parameters for $\pm 3\sigma = \pm 10\%$ at nominal (in $\mu W$).

| Statistics | Hybrid Model | |
|---|---|---|
| | Worst case design | Statistical design |
| Nominal leakage power | 9.17 | 9.17 |
| Distribution mean | 9.43 | 9.38 |
| Median | 8.90 | 9.37 |
| Std. deviation | 3.6919 | 0.2788 |
| Best leakage power | 2.13 | 8.44 |
| Worst leakage power | 39.4 | 10.58 |
| Variability (%) | 39.15 | 2.97 |

To determine the power budget of a circuit, all 6 process parameters are varied concurrently by $\pm 10\%$, and leakage power distributions are obtained by hybrid model based worst case and statistical design (Fig. 4, Table 2). Variability, expressed as a ratio of standard deviation to distribution mean ($\sigma/\mu$), is 39.15% for worst case design and 2.97% for statistical design. The predictability of worst to best corner leakage spread has improved by 95%, with a 13X reduction in $\sigma$, at an error in mean of less than 0.5%.

## 5 Conclusions

An optimal second order hybrid model is proposed for gate leakage power directly in terms of process parameters. It has been demonstrated that the hybrid model based statistical design results in considerable savings in the power budget of low power CMOS designs. This methodology is useful in bridging the gap between the Technology CAD and Design CAD through characterization of standard cell libraries for leakage power.

## References

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