Asymmetrical Triple-Gate FET

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Abstract

A novel triple-gate MOSFET structure with polysilicon gate process is proposed using asymmetrical (n^+/p^+) polysilicon gates. CMOS-compatible V_T's for high-performance circuit applications can be achieved for both nFET and pFET. The superior subthreshold characteristics and device performance are analyzed by three-dimensional numerical simulations. Comparisons of device properties with the mid-gap metal gate are presented.

1 Introduction

The triple-gate (TG) MOSFET has emerged as one of the promising candidates to extend CMOS technology beyond the scaling limit of conventional CMOS technology. The control of short-channel effects (SCEs) has become the major issue for device scaling beyond the 65 nm node [1]-[2]. In multi-gate FETs, thinning the channel film thickness is usually required yet challenging to suppress SCEs. Due to the superior SCEs, flexible body dimension, and manufacturability, the TG FET has been of much interest [1], [3]. Metal-gates with proper work functions, instead of channel doping engineering, have been employed to achieve the desired V_T in advanced multi-gate structures [4]. For CMOS application, two different work functions are usually required in order to balance the drive currents of nFET and pFET, which leads to technology complexity. In addition, gate work function engineering for multi-V_T design requires more exotic gate materials. This paper describes an asymmetrical (n^+/p^+) poly-gate structure for TG FinFET devices with CMOS-compatible V_T's using tilted implantations [5]-[6]. The device characteristics are analyzed using three-dimensional numerical simulations, and compared with metal-gate TG FinFET.

2 Proposed Device Structure

A novel TG FinFET structure compatible with the polysilicon process is proposed. In the conventional dual polysilicon CMOS technology (i.e. n+ and p+ polysilicon for nFET and pFET, respectively), the required channel doping density for TG devices has to be extremely high to achieve proper V_T (~0.2 V) or I_{off} (100 nA/μm), as indicated in Fig. 1. The proposed TG device structure with physically equivalent n^+-polysilicon gate and p^+-polysilicon gate is shown in Fig. 2(a). Two other possible structures with n^+/p^+ polysilicon gate offsets are shown in Fig. 2(b) and (c). The gate oxide surrounded by the gate has a uniform thickness (T_{ox}). The device structure under study has a cross-sectional body dimension of height (H_{Si}) and width (W_{Si}). Both H_{Si} and W_{Si} are assumed equal and are half of the effective channel length for proper SCE control. The total channel width can be defined as 2H + W. Multi-V_T options can be achieved using different patterns of the n^+/p^+ polysilicon.

We first assess the device I-V characteristics for the three gate structures, as compared with the mid-gap metal-gate device using a 3D numerical tool [7]. All the devices (nFETs) have the same L of 25 nm, T_{ox} of 1.3 nm, and thick buried oxide of 200 nm. In the simulations, Fermi-Dirac statistics, modified local density approximation for carrier confinement, and drift-diffusion transport model with field-dependent mobility were used. Fig. 3 shows the simulated I_{DS} vs. V_{GS} characteristics for the proposed structure (a) and mid-gap metal-gate device with comparable I_{off} (~50 nA/μm) set at V_{DS} = 1.1 V. To achieve the equal I_{off} value, a channel doping density of $7x10^{18}$ cm^{-3} is needed for the proposed structure, whereas an undoped body is used for the near-mid-gap metal-gate device. Due to higher mobility in the undoped channel, the mid-gap metal-gate device gives higher I_{on} (@V_{GS} = V_{DS} = 1.1 V). On the other hand, the proposed device exhibits better DIBL characteristics due to the higher vertical field attained by the positive back-gate filed in the asymmetrical device configuration as well as the use of the doped body. The proposed structures with different n^+/p^+ polysilicon gate offsets are compared in Fig. 4, which shows the simulated I_{DS} vs. V_{GS} characteristics for the three cases shown in Fig. 2. The same channel doping density ($7x10^{18}$ cm^{-3}) is used. Case (b) with larger p^+-polysilicon portion has the highest V_T, whereas case (c) with larger n^+-polysilicon portion has the lowest V_T. Fig. 5 further shows the I_{on} vs. I_{off} characteristics for the three poly-gate and the metal-gate devices. The three proposed structures offer a wide range of V_T selection, thus multiple V_T can be made.

The detailed device characteristics are listed in Table 1. The DIBL values of the proposed cases are much lower than that of the metal-gate device. Fig. 6 shows the inversion carrier distribution in the channel. The electron density is more uniformly distributed for the mid-gap metal-gate device, while it is crowded near the n^+-gate surface for the proposed structure (a) (results for structures (b) and (c) are not shown, yet similar). Hence, the proposed structures have improved DIBL's, as the carriers are better controlled due to the higher field perpendicular to the predominant n^+-gate.

Fig. 7 shows the I_{on} and I_{off} sensitivities to V_{DD}. As expected, I_{off} for structure (a) is slightly less sensitive than that of the mid-gap metal-gate device due to less DIBL. The I_{on} dependences on V_{DD} are similar for the three proposed structures, implying consistent dynamic power scaling when these structures are integrated on the same chip for multi-V_T design. The DIBL advantage is further reflected in Fig. 8. To gain insight into CMOS circuit speed performance, we also simulated C-V characteristics, as shown in Fig. 9, for CV/I comparison. The CV/I_{on} value of our proposed structure (case (a)) is about 50% (at V_{DD} of 1.1V) higher than that of the mid-gap metal-gate one mainly due to lower I_{on}. However, as V_{DD} is decreased, the gate capacitance for the proposed scheme decreases faster and hence it is more suitable for low-voltage applications.

3 Conclusion

A novel TG MOSFET structure using asymmetrical polysilicon gates is proposed. Due to the superior SCEs, the proposed TG device offers better channel length scalability compared with TG devices with near-mid-gap metal-gates. By changing the patterns/offsets of the n^+/p^+ polysilicon gates, multiple V_T can be achieved. Hence, this structure can be used in low-power high-performance VLSI.

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References

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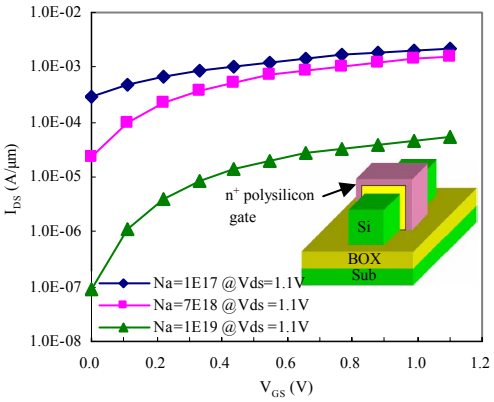

Figure 1: Taurus-simulated I_{DS} vs. V_{GS} characteristics for a TG nMOSFET with n^+ polysilicon gate and different dopings (N_a's). The inset shows the 3-D structure (not to scale) for simulation (L = 25 nm, gate oxide = 1.3 nm, silicon height = silicon width = 12.5 nm).

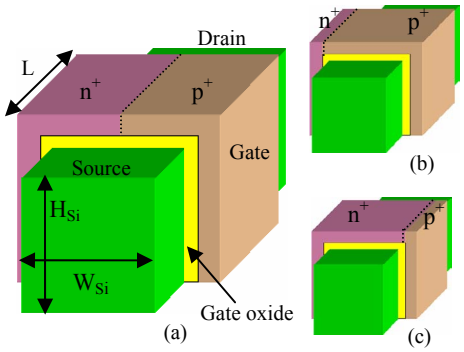

Figure 2: 3-D view of the proposed triple-gate structures (a), (b), and (c) with different n^+/p^+ polysilicon gate offsets. (The thick buried oxide (BOX) layer underneath is not shown for brevity.)

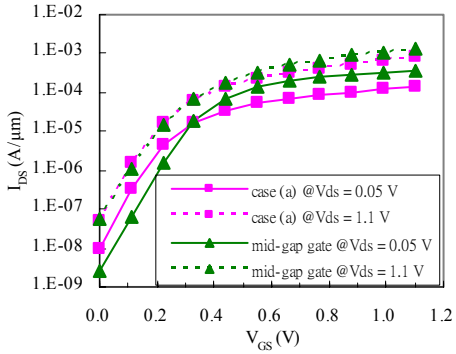

Figure 3: Taurus-simulated I_{DS} vs. V_{GS} characteristics for the proposed structure (a) and the mid-gap metal-gate device with comparable I_{off} (~50 nA/μm) set at V_{DS} = 1.1 V.

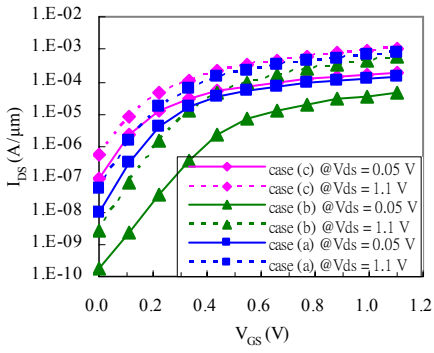

Figure 4:. Taurus-simulated I_{DS} vs. V_{GS} characteristics for the three proposed structures.

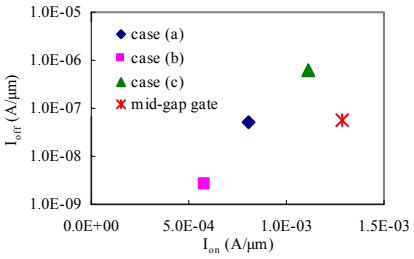

Figure 5: I_{on} vs. I_{off} for the proposed structures and the near-mid-gap metal-gate device.

Device type	Mid-gap gate	Case (a)	Case (b)	Case (c)
$V_{T(sat)}$ (V)	0.16	0.15	0.27	0.08
I_{off} (A/μm)	5.76 x10^{-8}	5.16 x10^{-8}	2.52 x10^{-9}	5.34 x10^{-7}
I_{on} (A/μm)	1.29 x10^{-3}	8.05 x10^{-4}	5.80 x10^{-4}	1.05 x10^{-3}
I_{eff} (A/μm) [8]	7.77 x10^{-4}	4.74 x10^{-4}	3.05 x10^{-4}	6.40 x10^{-4}
DIBL (mV/V)	101	50	82	54
Sub. Swing (mV/dec)	90	81	79	89
CV/I_{on} normalized	1	1.49	2.00	1.20

Table 1: Predicted device characteristics of the proposed and mid-gap metal-gate devices for comparison (V_{DD} = 1.1 V). $V_{T(sat)}$ was extracted by constant current method (0.1 μA x (W/L) at $V_{DS} = V_{DD}$).

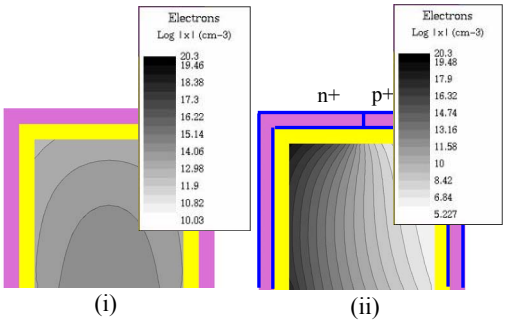

Figure 6: Electron distribution in the cross section cut at mid-channel for (i) the mid-gap metal-gate device, and (ii) the proposed structure (a) ($V_{GS} = V_{DS} = 0$ V).

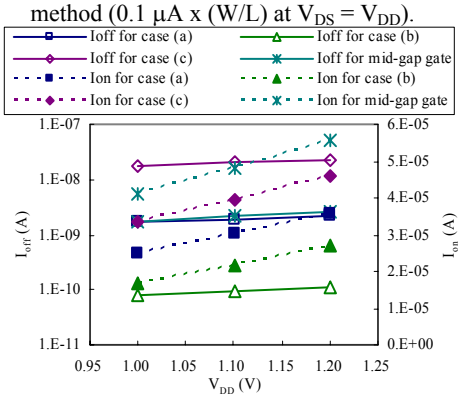

Figure 7: Predicted I_{on} and I_{off} sensitivities to V_{DD}.

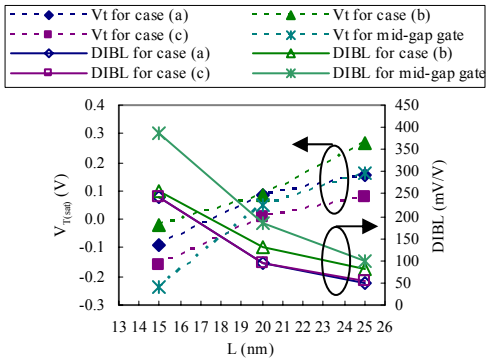

Figure 8: Predicted $V_{T(sat)}$ and DIBL vs. L scaling.

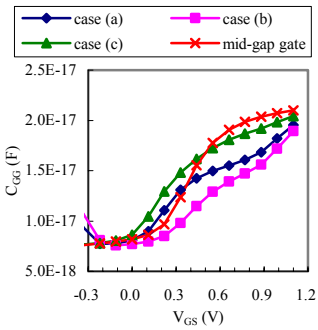

Figure 9: Predicted C-V characteristics.