SIMULATION OF SEMICONDUCTOR PROCESSES AND DEVICES Vol. 12
Edited by T. Grasser and S. Selberherr - September 2007

Simulation of Analog/RF Performance and Process Variation in Nanowire Transistors

Runsheng Wang, Jing Zhuge, and Ru Huang

Institute of Microelectronics, Peking University, Beijing 100871, China
ruhuang@pku.edu.cn

Abstract

In this work, the RF performance of Si nanowire transistors (SNWTs) is computationally investigated, including RF figures of merit, impacts of parasitic effects and nanowire cross-sectional shape fluctuation caused by process variation. The simulated results show superior RF scalability of SNWTs and severe impacts of parasitic capacitance and process fluctuations. The influence of gradient doping profile in source/drain extension region of SNWTs on RF application is also studied.

1 Introduction

Recently, the Si nanowire transistor (SNWT) (as schematically shown in Fig. 1) has received a lot of attentions as one of the promising candidates for future CMOS technology [1-3]. Most reported simulation work have focused on the SNWT's DC characteristics [4,5]. Their potentials in RF application have seldom been studied. In addition, extrinsic parasitic impacts in such small devices and intrinsic parameter fluctuations caused by process variation have emerged as major scaling limitations for nanodevices. The RF figures of merit (FoMs), the impacts of parasitic effects and process variations on RF performance of SNWTs and influence of doping profile in source/drain extension (SDE) region on RF application are computationally investigated in this work.

2 Simulation Methodology

First, by carefully tuning in mobility model and 3-D density-gradient quantum correction drift-diffusion model, the DC solution of the commercial TCAD tool [6] was calibrated with the results simulated by 3-D full quantum mechanical models [4]. As shown in Fig. 2, the transfer characteristics of cylinder gate-all-around nanowire MOSFET can be well reproduced under careful parameter modification. Based on this, the modified simulator was then applied for the AC device simulation to extract the Y-parameters of SNWTs. As will be presented below, the simulation can well predict the main tendency of RF properties for the examined SNWT device structure.

3 Results and Discussion

The central FoMs of RF technology are the cutoff frequency f_t and maximum oscillation frequency f_{max}. The FoMs investigated here are at the drain bias V_d=V_{dd}=0.4V and overdrive gate bias (V_g−V_t) of 0.1V, which is a good compromise between speed and power consumption.

3.1 Intrinsic RF performance

The simulation results demonstrate that SNWTs can show superior RF scaling capability. With the downscaling of the gate length (L_g), the f_t of SNWTs will highly increase. It is also shown in Fig. 3 that the f_t increases with decreasing t_{si}, due to decreasing capacitance and increasing g_m ($f_t \approx g_m/C_g$). It can be concluded from the intrinsic characteristics that the SNWT is suitable for low-power RF circuits design.

3.2 Impacts of Parasitic Effects

The main parasitic factors are source/drain contact resistance and parasitic outer-fringing capacitance between gate and source/drain (the gate-height is chosen as $2L_g$ [1]). As shown in Fig. 4, the parasitic impacts on f_t are quite small due to its insensitivity to resistance ($f_t \approx g_m/C_g$). However, f_{max} of SNWTs is much dependent on extrinsic elements ($f_{max} \approx f_t/2((R_s+R_g)(g_{ds}+g_m/(C_{gs}/C_{gd}+1)))^{1/2}$ [7]). Thinner SNWT (i.e., smaller t_{si}) is more sensitive to parasitic capacitance than parasitic resistance, while thicker SNWTs are opposite. It can also be observed from the figure that the parasitic outer-fringing capacitance is the dominating factor in RF application of SNWTs due to the ultra-small intrinsic capacitance of nanowire.

3.3 Impacts of Process Variations

Three types of nanowire cross-sectional shape fluctuation caused by process variation are computational estimated in terms of nanowire diameter t_{si}, elliptical shape and corner rounding, as shown in Fig. 5 to Fig. 7. However, the results show that the impacts on fluctuations of intrinsic f_t and f_{max} are relatively severe, which suggest special design should be made for robust RF applications. It also indicates that, for SNWTs with $t_{si} \geq$ 4nm, the acceptable process variation tolerance for RFIC design is: Δt_{si} <1nm, $\Delta t_{ma}/2$ <0.4nm and r/R >75%.

3.4 Effects of Doping Profile in SDE Region

In this section, the RF performance of SNWTs with gradient doped SDE is studied. Gaussian profile is adopted (Fig. 8), and σ is the standard deviation of the doping profile. Increasing σ (i.e., more gradient doping profile) will result in smaller resistance but larger parasitic capacitance, which indicates a tradeoff in RFIC design. As shown in Fig. 9, f_t of SNWTs is less influenced by SDE doping variations, while the f_{max} shows much distinct dependence on the doping profile in SDE region. With increasing σ, the f_{max} of SNWTs increase in initial stages and then degrade beyond a turning point, which due to the competition between the opposite impacts of resistance and capacitance, as shown in Fig. 10. And the turning point is more delayed with thinner SNWT due to its larger intrinsic resistance, which suggests special design can be made.

4 Conclusion

In this paper, the RF performance of SNWTs is computationally investigated. The results indicate that SNWTs exhibit superior intrinsic RF scaling capability and are

suitable for low-power RF applications. The impacts of parasitic effects and nanowire shape fluctuation caused by process variation are studied and found to be relatively severe, and the acceptable design region of parameters for RFIC design is given. The effects of SDE doping gradients are also investigated, which give additional design considerations.

Acknowledgements

This work was partly supported by the collaborative project between Samsung Electronics Co. and PKU, the NSFC (60625403), 973 Program, and the NCET Project.

References

[1] http://public.itrs.net. [2] Y. Cui et al., *Nano Lett.*, vol. 3, no. 2, p. 149, 2003. [3] F.L. Yang et al., *Symp. on VLSI Tech.*, p. 196, 2004. [4] J. Wang et al., *J. Appl. Phys.*, vol. 96, no. 4, p. 2192, 2004. [5] M. Bescond et al., *IEDM*, p. 617, 2004. [6] TCAD Sentaurus Device user's manual, Synopsys, 2005. [7] H. S. Bennett et al., *IEEE Trans. Electron Devices*, vol. 52, no. 7, p. 1235, 2005. [8] F. Schwierz et al., *Microelectron. Reliab.*, vol. 47, no. 2/3, p. 384, 2007.

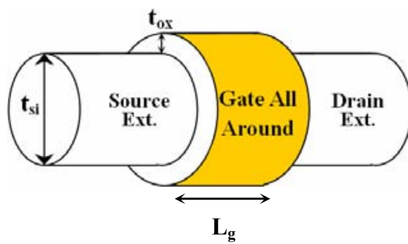

Figure 1: Schematic view of the simulated SNWT structure.

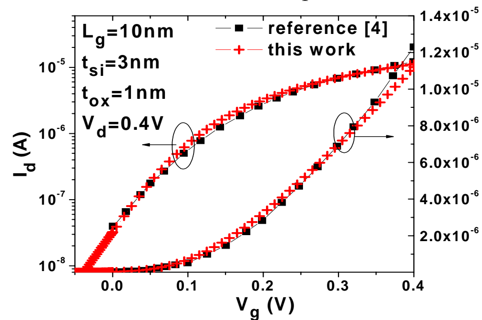

Figure 2: Simulated transfer characteristics of a SNWT in this work.

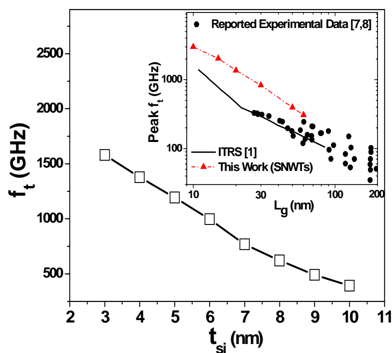

Figure 3: f_t of intrinsic SNWTs with different diameters. Inserted show peak f_t values of SNWTs as a function of L_g, compared to the reported experimental data of other MOSFET types [7,8] and ITRS requirement [1].

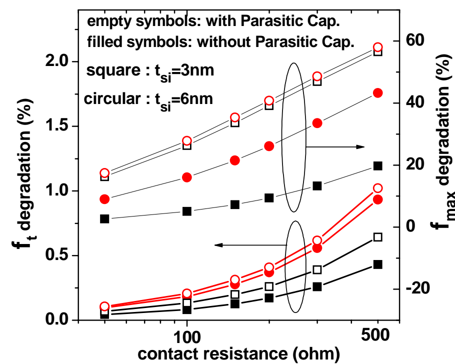

Figure 4: Impacts of parasitic contact resistance and parasitic outer-fringing capacitance on f_t and f_{max} degradation of SNWTs with different diameters.

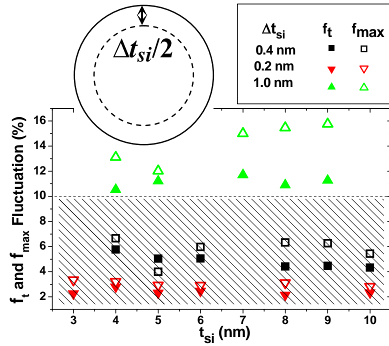

Figure 5: Impact of t_{si} fluctuation on f_t and f_{max} of SNWTs.

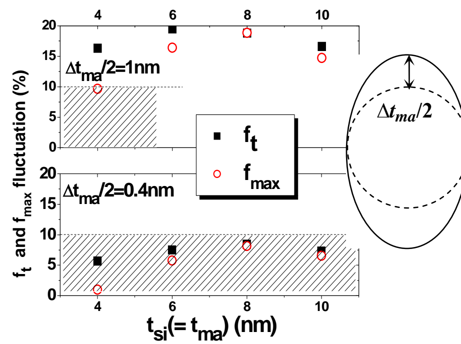

Figure 6: Impact of ellipses variation (t_{ma}) on f_t and f_{max} of SNWTs.

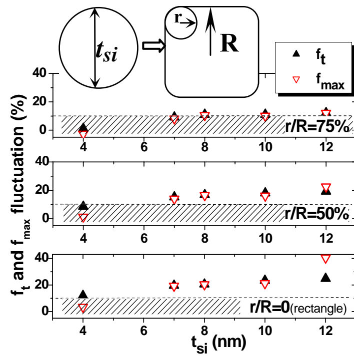

Figure 7: Impacts of corner rounding variation on f_t and f_{max} of SNWTs.

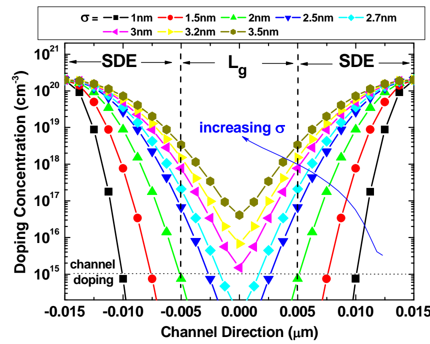

Figure 8: SDE doping profile variation of SNWTs with L_g=10nm. σ is the standard deviation of the Gaussian doping profile adopted.

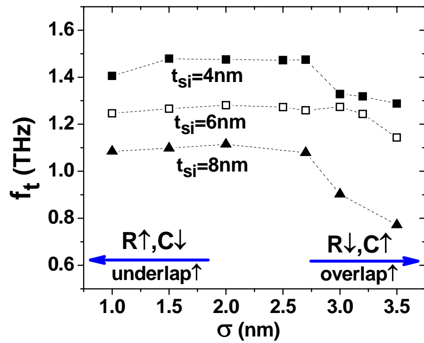

Figure 9: Impacts of various SDE doping gradients on f_t of SNWTs. σ is illustrated in Fig. 8.

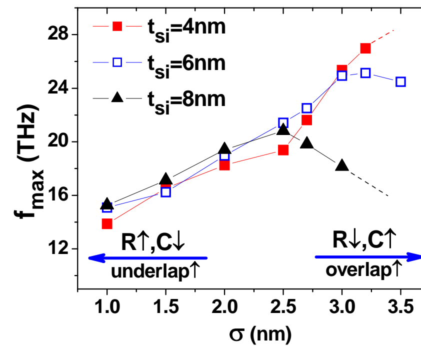

Figure 10: Impacts of various SDE doping gradients on f_{max} of SNWTs. σ is illustrated in Fig. 8.