Hot-Carrier Behaviour of a 0.35 µm High-Voltage n-Channel LDMOS Transistor

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Abstract

This paper describes the hot-carrier (HC) behaviour of a high-voltage 0.35 µm n-channel lateral DMOS transistor (LDMOSFET). Self-heating effects during HC stress have to be taken into account for the HC stress analysis. Peak I_{dlin} and I_{dsat} degradations were observed at the stress bias V_G = 0.8 V and V_G = 2.5 ~ 3.0 V, respectively. Together with TCAD simulations and measurements, one can clearly explain the HC effects occurring near the bird's beak region and show their impact on the I_{dlin} and I_{dsat} degradations.

1. Introduction

High-voltage (HV) LDMOSFETs are widely used for output stage devices in smart power applications. Considerable effort has been put into the development of LDMOSFETs for automotive electronics, computer peripheral appliances, and portable equipment, such as cellular phones [1-2]. The main issues in the development are to obtain the best trade-off between specific on-resistance R_{SP} and breakdown voltage BV, and to shrink the feature size without degrading device characteristics [3-4]. However, HC related reliability is one of the limiting factors in practical applications. The high electric field near the bird's beak region is believed to be a major cause of the HC generation. One can see a peak electric field at the bird's beak region in the blocking case or with low gate voltage. With increased gate voltage the peak electric field moves from the bird's beak towards the drain side, and HC generation at the bird's beak region is suppressed at high gate voltages. HC generate defects in the oxide and at the Si/SiO_2 interface. Interface traps (or charge trapping in the oxide) created by this process collect charge over time and directly affect the device operation [5]. Two-dimensional device simulations (DESSIS) together with measurements are performed to explain clearly the HC behaviour of a HV n-channel LDMOSFET including self-heating effects.

2. Simulation and experiments

The device was fabricated in a 0.35 µm CMOS-based HV technology. Gate oxide thickness of 7 nm was formed by thermal oxidation. A HV n-channel LDMOSFET for 50 V applications, with a gate length of 0.5 µm and a width of 40 µm, was used in

the study. HC stress experiments were performed at V_G from 0.8 V to 3.0 V, and V_D = 50 V for device reliability evaluations. Device simulations (Fig. 1) with the commercial device simulator DESSIS from Synopsys, clearly show a peak location of the impact-ionization and the direction of the electric field E_n normal to the current flow at the Si/SiO_2 interface. Near the bird's beak region, there are two adjacent regions which show electric field components normal to the current flow vector, near the Si/SiO_2 interface, with a positive and a negative sign respectively. Consequently, both cases of electron and hole injection have to be considered for I_{dlin} and I_{dsat} degradation behaviour.

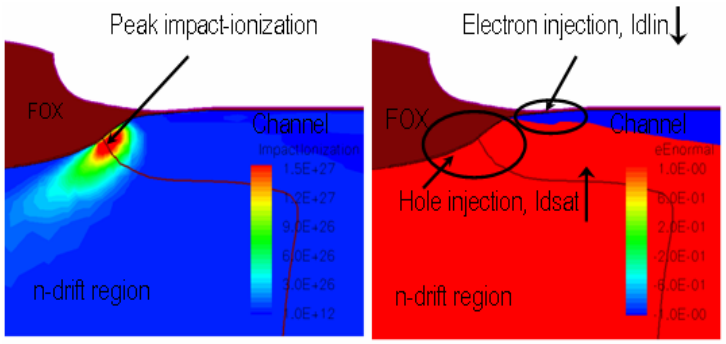

Fig. 1: Impact-ionization (left) and a normal component of electric field E_n (right) at V_G = 1.2 V and V_D = 50 V.

ΔI_{dlin} (degradation of the linear current) shows a peak at the stress bias V_G = 1.2 V (Fig. 2). On the other hand, the highest peak ΔI_{dsat} (degradation of the saturation current) is observed under the stress at high V_G. Assuming donor and acceptor traps (pre-existing prior to stress) at the bird's beak region, I_{dlin} decreases with electron injection (or trapping at the acceptor states). I_{dsat} increase can be explained by donor type interface trap generation (or hole trapping in the oxide), which corresponds to the fact that the negative charge by the electron injection is compensated by the positive charge build-up at the Si/SiO_2 interface and in the oxide (Fig. 3).

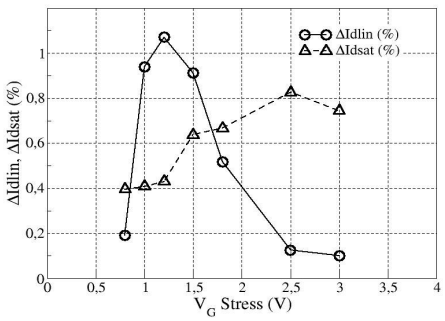

Fig. 2: ΔI_{dlin} and ΔI_{dsat} versus V_G stress with fixed V_D = 50 V, and stress time at 1e4 sec.

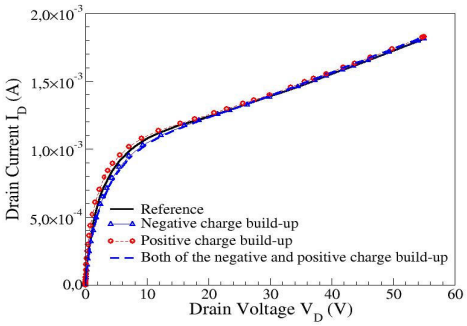

Fig. 3: I_D versus positive and negative charge build-up at the Si/SiO_2 interface and in the oxide.

Fig. 4 shows a steep temperature increase by the self-heating during HC stress at V_G = 3.0 V and V_D = 50 V. HC stress was done with the device in on-wafer measurements, and it's a challenge to set the thermal boundary conditions for TCAD simulations correctly. Thermal resistance R_{th} in Fig. 4 can be extracted from the DC IV curves at different ambient temperature [6]. Temperature distribution inside a device due to self-heating is determined by the heat generation profile and the thermal conduction of the device. In majority carrier devices such as MOSFETs, there is very little carrier recombination and as a result heat generation is mainly caused by Joule heating, which is proportional to the local resistances of the drift and channel regions. As shown in the figure, the bottom of the device was assumed to have an R_{th} = 0.0755 cm^2 K/W, which was calibrated with the substrate thickness about 700 µm and a width of 700 µm where it was assumed that the gradient of the temperature profile diminishes. The temperature rise is highest in the middle of the drift region (470 K), and it decreases towards the bottom of substrate (341 K). The channel region also shows a high temperature from 448 K to 460 K.

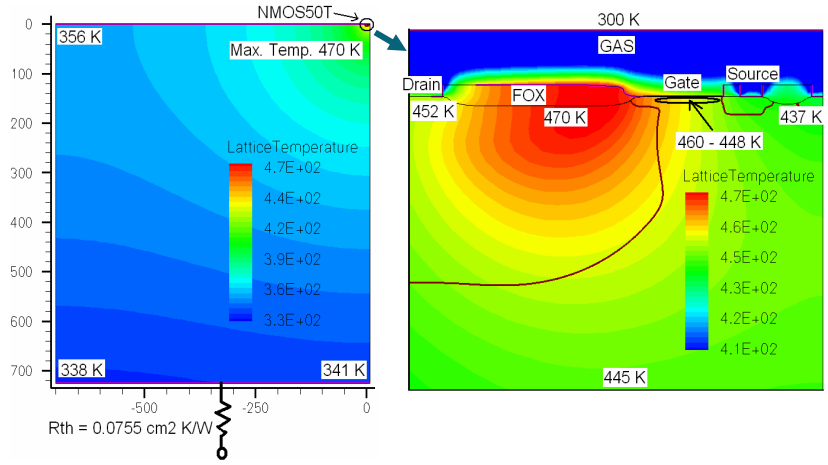

Fig. 4: Temperature distribution at V_G = 3.0 V and V_D = 50 V. R_{th} = 0.0755 cm^2 K/W was assumed with a device which shows a gate length = 0.5 µm and a width = 40 µm.

Fig. 5 shows the extracted channel temperature from the DC IV measurements. Channel width also affects the temperature rise of the device, and it was taken into account for R_{th} calibration too. Indirectly measured channel temperature 470 K = 300 K + 170 K in Fig. 5 shows a good match with a simulated channel temperature 448 ~ 460 K in Fig. 4. In our devices V_{th} shifts were found to be negligible. However, I_{dlin} and I_{dsat} degradations were observed under the HC stress, which correspond to a charge build-up at the $Si/Si0_2$ interface and in the oxide near the bird's beak region. Fig. 6 shows the lifetime (at 1 % R_{on}) versus V_G stress. Lifetime increases at high V_G stress. I_{dlin} directly affects the R_{on}, and I_{dlin} degradation by the HC generation at the bird's beak region is reduced with increased gate voltage. Because the peak electric field is moved towards drain contact self-heating effects further suppress the HC generation of the device.

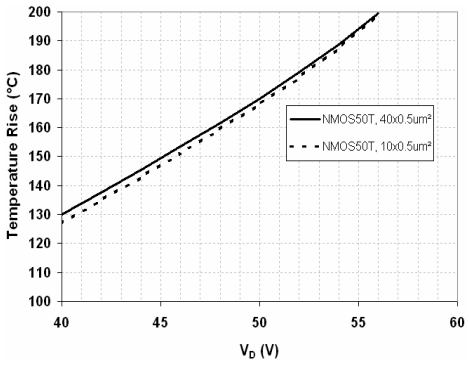

Fig. 5: Temperature rise at the channel region at $V_G = 3.0$ V and $V_D = 40 \sim 55$ V (calculated from the measurements).

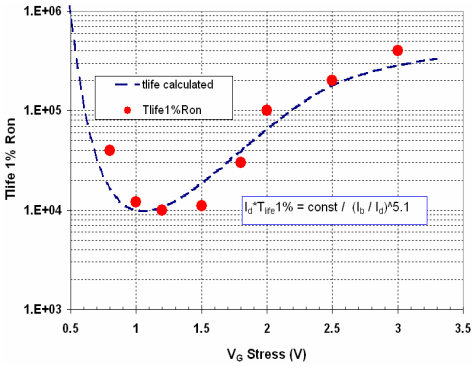

Fig. 6: Life time (at 1% R_{on}) versus V_G stress ($V_D = 50$ V).

3. Conclusion

HC behaviour of a HV n-channel LDMOSFET was studied with 2D device simulations and measurements. A large amount of temperature increase by the self-heating was observed during HC stress at $V_G = 3.0$ V and $V_D = 50$ V. The thermal resistance R_{th} for TCAD simulations was calibrated from the DC IV measurements. TCAD simulations show that both of the electron and hole injections at the bird's beak region have to be considered for I_{dlin} and I_{dsat} degradations.

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