Efficient Green's Function Algorithms for Atomistic Modeling of Si Nanowire FETs

A. Pecchia*, G. Penazzi*, A. Di Carlo*
*Department of Electronics and Electrical Engineering,
University of Rome "Tor Vergata", Via del Politecnico 1, 00133, Roma, Italy
pecchia@ing.uniroma2.it

Abstract

Atomistic simulations of transport properties of an ultra-scaled silicon nanowire (SiNW) field-effect transistor (FETs) in a Gate-All-Around configuration are reported. The calculations have been obtained using a semi-empirical tight-binding representation of the system Hamiltonian based on first-principles density functional theory (DFT). An efficient non-equilibrium Green's functions (NEGF) scheme has been implemented in order to compute self-consistently the charge density and the electrostatic potential in the SiNW channel.

1 Introduction

Silicon nanowire (SiNW) FETs are promising candidates as extremely down-scaled MOSFETs to replace traditional bulk-devices, since they can be synthesised and assembled with controlled and predictable composition, diameter, length and doping. The system we have simulated is a ultra-scaled *pip* gate-all-around (GAA) SiNW FET [1], shown in Fig. 1. An efficient implementation of the non-equilibrium Green's function algorithm with liner scaling properties has been implemented in order to tackle this problem. The method allow atomistic computations of relatively long wires.

2 Efficient matrix Green's function algorithm

All results presented in this work have been obtained using the quantum transport simulator *g*DFTB [2] which is an extension to transport applications of the *density func*

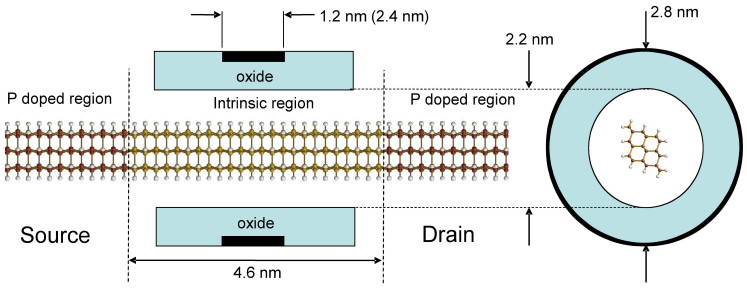

Figure 1: Representation of a simulated Si[110] nanowire *pip* FET device.

tional tight binding (DFTB) method [2]. The essence of DFTB is of providing a physically sound representation of the tight-binding parameters used to construct the system Hamiltonian based on first-principle DFT calculations. In DFTB the degree of sparsity of the matrices is generally larger than in empirical TB, since the interactions extends to 2^{nd} and sometimes to 3^{rd} nearest neighbouring atoms. Furthermore, beside the TB Hamiltonian (H), also the overlap (S) between atomic orbitals must be considered. The *g*DFTB code implements the non-equilibrium Green's functional (NEGF) scheme which is used to compute self-consistently the charge density and the electrostatic potential within the device. The NEGF method has been extensively described and discussed in the literature [3]. The advantage of NEGF is that open boundary conditions can be elegantly included by exactly mapping the contacting leads into a finite and small part of the system via *self energies* [3], and scattering mechanisms can be easily included in a fully consistent approach. The draw-back of the method resides in its computational burden and delicate convergence. The key ingredient is the *retarded* GF, G^r, defined as $G^r(E) = [ES - H + \Sigma^r(E)]^{\ 1}$, and $\Sigma^r(E)$, the contact self-energy [3]. In quasi one-dimensional systems, the atoms can be arranged into layers, such that H and S take the block tridiagonal form. The diagonal blocks can have different sizes but must have all a square shape. The corresponding layers are called *principal layers* (PL) and have the property that the interaction of each PL is restricted to two nearest neighbours PLs. This structure can be exploited by devising an efficient computation of the Green's function. Indeed, the direct inversion of the whole Hamiltonian can be extremely time consuming for large structures. In general the Green's function does not preserve the block tridiagonal structure, but only the sub-blocks where the matrix S is non-vanishing are actually needed in order to compute the charge density. This is a direct consequence of the limited extension of the overlap between atomic wavefunctions. The GF is computed using a block-iterative algorithm similar to that of Ref. [4] but adapted to semi-empirical TB including the overlap matrix. The mathematical details will be discussed elsewhere. The charge density is obtained by appropriate integration over energy of $G^r(E)$ [3]. The Poisson equation is solved using a 3D multigrid algorithm that can implement generally complex potential boundary conditions such as planar or cylindrical gates [2]. The latter configuration is used to simulate the GAA-SiNW.

3 Model and Results

In this work we report calculations performed on a H-terminated SiNW oriented along the [110] direction and having about 1 nm in diameter. The choice of growing direction is supported by experimental evidences, showing that the [110] direction is preferred for diameters smaller than 10 nm [5]. The electrostatic controlling parameters governing the characteristics and trans-characteristics behaviour of the device can be understood from the equivalent circuit model similar to [6], where the total capacitance of the gated SiNW, C_{tot}, is the series connection of the geometric (C_G) and the quantum capacitance (C_Q). These capacitances are calculated with our atomistic tool as a function of the device geometry and doping concentration. This allows a detailed analysis of the ultra-short channel *pip* SiNW device which emphasise the role of a correct choice of both the doping-profile and the gate parameters in order to improve the transistor perfor-

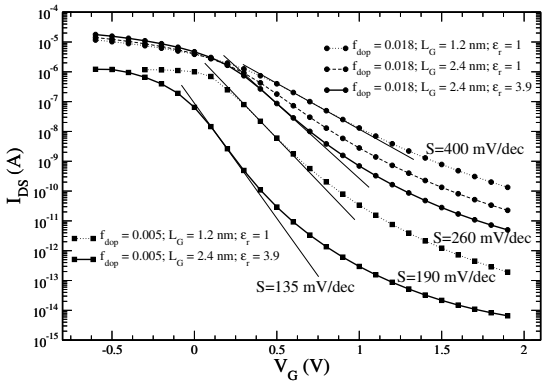

Figure 2: Comparison of *pip* device trans-characteristics for different doping, gate lengths and dielectric constants.

mance. Figure 2 reports the trans-characteristics behaviour of the device for different doping concentrations of the contacts and two different gate-lengths of 1.2 nm and 2.4 nm. Results for a low (p=0.005 holes/Si, $N_A = 2.3 \cdot 10^8\ cm^{\ 1}$) and a high ($p$=0.018 holes/Si, $N_A = 8.4 \cdot 10^8\ cm^{\ 1}$) p-doping concentrations are reported. Increasing the gate-length increases the gate capacitance of the device, with a corresponding improvement of gate control and subthreshold slope. At low temperatures a subthreshold slope of 135 mV/dec is found for a gate length of $L_G = 2.4nm$. Increasing the doping fraction has the effect of increasing the output current, but considerably increases the subthreshold slope. This effect is correlated to the fact that the built-in potential barrier does not increase proportionally with doping because charge-transfer to the intrinsic channel is limited by the short channel length and by the quantum capacity of the SiNW. As a consequence, for larger p, the Fermi level in the degenerate p-doped contacts approaches the top of the barrier and for very large doping fractions can even be higher, leading to large off-currents due to over-the-barrier ballistic conduction. The current switching are also explored in a fully self-consistent, temperature-dependent calculation shown in Figure 3. Also in this case different behaviours are found for the high and low p-doping regimes. For low doping, as temperature increases, the tunnelling current slightly increases and the sub-threshold swing deteriorates. On the contrary, in the high p-doping regime, the trans characteristics, although much higher, are found practically independent of temperature. This is due to the fact that in the high p-doping regime the thermionic current is insensitive of temperature variations. This could be an advantage in ultra-scaled FET design. The gate delay can be estimated from $\tau = C\Delta V / I_{on}$. Assuming a voltage swing, ΔV, of about 1 V in order to obtain a ratio $I_{on}/I_{off} \approx 10^5$, a load capacitance of 0.3 aF and a current $I_{on} \approx 1\mu A$, we obtain a gate delay of 0.3 ps. At the expenses of a much lower ratio $I_{on}/I_{off} \approx 10^3$ the gate delay can be reduced by about one order of magnitude. These values are in agreement with the trend shown by Si nanodevices of comparable gate lengths.

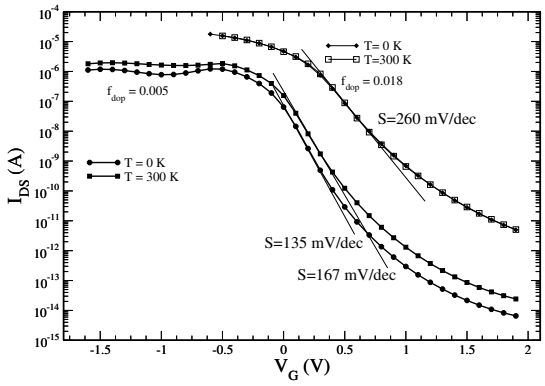

Figure 3: Temperature dependence of the trans-characteristics.

4 conclusions

A detailed analysis of a ultra-short channel *pip* GAA SiNW device have been reported, emphasising the role of both the doping-profile and the gate parameters in order to improve the transistor performance. A low temperature subthreshold slope of 135 mV/dec is found for a gate length of $L_G = 2.4nm$. For the same device the gate delay is of the order of 0.3 ps. These values are found in agreement with the trends of Si devices. In the low p-doping regime, as temperature increases the tunnelling current increases and the sub-threshold swing slightly deteriorates. On the contrary, in the high p-doping regime, the trans characteristics are found practically insensitive of temperature.

References

[1] N. Singh, A. Agarwal, L. K. Bera, T. Y. Liow, R. Yang, S. C. Rustagi, C. H. Tung, R. Kumar, G. Q. Lo, N. Balasubramanian, and D.-L. Kwong, "High-performance fully depleted silicon nanowire (diameter = 5 nm) gate-all-around cmos devices," *IEEE Elect. Dev. Lett.*, vol. 27, p. 383, 2006.

[2] A. Pecchia, L. Latessa, A. Gagliardi, T. Fraunheim, and A. Di Carlo, *Molecular and Nano electronics: analysis, design and simulations*. New York: Elsevier, 2006.

[3] S. Datta, "Nanoscale device simulation: The green's function formalism," *Superlattices and Microstructures*, vol. 28, p. 253, 2000.

[4] R. Lake, G. Klimeck, R. C. Bowen, and D. Jovanovic, "Single and multiband modeling of quantum electron transport through layered semiconductor devices," *J. Appl. Phys.*, vol. 81, p. 7845, 1997.

[5] Y. Cui, L. J. Lauhon, M. S. Gudiksen, J. Wang, and C. M. Lieber, "Diameter-controlled synthesis of single-crystal silicon nanowires," *Appl. Phys. Lett.*, vol. 78, p. 2214, 2001.

[6] L. Latessa, A. Pecchia, A. Di Carlo, and P. Lugli, "Atomistic modelling of carbon nanotube field-effect transistors," *IEEE Trans. Nanotechnol.*, vol. 6, p. 13, 2007.