

Calibrated Hydrodynamic Simulation of Deeply-Scaled Well-Tempered Nanowire Field Effect Transistors

O.M. Nayfeh and D.A. Antoniadis

Department of Electrical Engineering, Microsystems Technology Laboratory,
Massachusetts Institute of Technology
onayfeh@mtl.mit.edu

Abstract

In this work, we first extract Hydrodynamic (HD) parameters from a computationally intensive full-band Monte Carlo (MC) solution via the MOCA simulator. We are then able to achieve good fits between the calibrated HD and MC velocity profile of a near ballistic double gated FET (DGFET). Moreover, we demonstrate good fits using bulk-Si HD parameters between the I-V characteristics of HD simulation and the measured data of deeply scaled Silicon nanowire field effect transistors (SNWFETs).

1 Introduction

Silicon nanowire FETs have recently been fabricated by both bottom-up and top-down processes. Top-down CMOS fabrication via conventional lithography of gate-all-around (GAA) Si nanowire field effect transistors (SNWFETs) with physical 15 nm gate length, 8 nm wire diameter, and 3.5 nm oxide thickness have also been recently been fabricated and measured in [1]. The measured data exhibits the promising characteristics of a 22-nm-CMOS-node and below technology- near ideal sub-threshold swing (SS), extremely small drain dependence of V_t (i.e. small DIBL), and good current drive (I_d). Moreover, the data provides an excellent platform for the testing, calibration, and benchmarking of simulation models applicable for NWFETs. The design and optimization of these promising devices requires accurate, fast, and efficient simulation models. The hydrodynamic transport (HD) model has been used extensively in the sub 0.1 μm regime, however, there is debate on the validity of HD in the sub-50 nm near ballistic transport regime [2].

2 Hydrodynamic Model Calibration

Previously, we calibrated the scattering rates of MOCA [3] from measured drive current data of a well-tempered $L_{\text{eff}}=35$ nm bulk-Si nFET that operates at $\sim 50\%$ of the thermal limit [4]. MOCA includes quantum correction to the charge density via Schroedinger-Poisson. We extract an

energy relaxation time, $\tau_E = 0.1$ ps from a local balance equation, and averages over the distribution function as in [5]. We also extract the energy flux parameter $r_n = 0.3$ from a plot of S vs. VW , where S is the energy flux, V is the average velocity, and W is the average energy [5]. These parameters are imported into the DESSIS continuum simulator, and differ from larger default values of $\tau_E = 0.3$ ps, and $r_n = 0.6$. We extended the MOCA simulation to near ballistic DGFETs. **Fig. 1** shows a DGnFET that operates at $\sim 80\%$ of the thermal limit ($L_{\text{gate}} = 9$ nm, $T_{\text{si}} = 4$ nm, $T_{\text{ox}} = 1$ nm, “equivalent mobility” μ for a long-channel device $= 250$ cm²/Vs [6]). We extract from MOCA $\tau_E = 0.14$ ps, and $r_n = 0.3$ [5]. We find that for $T_{\text{si}} > 5$ nm, τ_E approaches the bulk 0.1 ps. More accurate QM correction for MC is needed to properly evaluate sub-5 nm films [7]. **Fig. 2.** shows the velocity profile fits between MOCA and HD of this DG FET. The HD simulation uses the density-gradient model (DG) for quantum correction and matches the MOCA charge distribution well. As can be seen, calibration of only τ_E still results in source velocity $v_{\text{inj}} = 1.25 \times 10^7$ cm/s at the peak of the potential barrier x_0 that still exceeds that of MOCA, 0.85×10^7 cm/s. However, after also calibration of r_n , a good match is now achieved for v_{inj} .

2.1 Hydrodynamic Simulation of Silicon Nanowire FETs

Fig. 3. shows a schematic of a 3D GAA Si NW FET. The key parameters are the gate length = 15 nm, source/drain extension length = 15 nm, oxide thickness = 3.5 nm, and S/D doping gradient = 2 nm/dec. **Fig. 4a** demonstrates good fits for the drain current on a linear-scale plot for the low ($V_{\text{ds}} = 50$ mV) and high ($V_{\text{ds}} = 1.0$ V) drain bias via HD simulation using the bulk-Si parameters, ($\tau_E = 0.1$ ps, $r_n = 0.3$) and a constant “equivalent mobility” of 275 cm²/Vs. QM correction is via the DG model which has efficient convergence with HD. **Fig. 4b** shows I-V fits on a log plot. As can be seen the near SS, and low DIBL are captured well. In conclusion, we demonstrate the applicability of HD simulation of near-ballistic FETs with calibrated parameters from Monte-Carlo. Future work will involve calibration to NWFET data with sub-5 nm wire diameter, as data and more accurate QM correction to particle-based Monte-Carlo becomes available.

Acknowledgements

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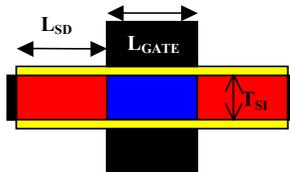


Figure 1: Near Ballistic Double-Gated FET Structure

Lgate=Lsd (nm)	Tsi (nm)	Tox (nm)	Vdd (V)	Equivalent μ (cm ² /Vs)
9	4	1	0.8	255

Table 1: Near Ballistic Double-Gated FET parameters

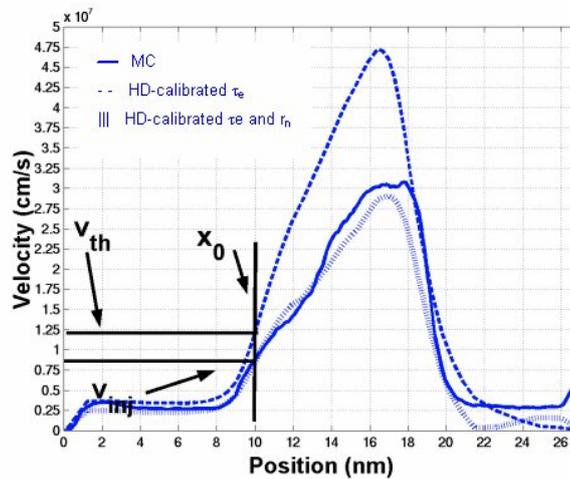


Figure 2: Velocity profiles for a cut in the center of the channel between full-band MC (MOCA) and HD of a $L_{gate}=9$ nm, $T_{si}=4$ nm double-gate FET that operates at 80% of the thermal limit. Shown is the HD profile with only calibration of the energy relaxation time ($\tau_e=0.14$ ps, $r_n=0.6$) in which the HD source velocity $v_{inj}=1.2 \times 10^7$ cm/s

at the peak of potential barrier x_0 still exceeds the MOCA source velocity $\sim 0.85 \times 10^7$ cm/s. Also shown is HD with calibrated energy relaxation time, and energy flux parameter ($\tau_e=0.14$ ps, $r_n=0.3$) which now produces a good match to the MC source velocity.

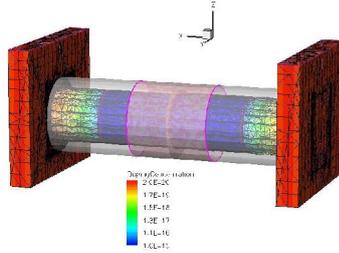


Figure 3: Schematic of 3D GAA Si nanowire FET. The relevant parameters are the gate length ($L_{\text{gate}}=15$ nm), wire diameter ($d_{\text{wire}}=8$ nm), source/drain extension length ($L_{\text{sd}}=15$ nm), oxide thickness ($T_{\text{ox}}=3.5$ nm), and S/D doping gradient ($\sigma_{\text{sd}}=2$ nm/decade).

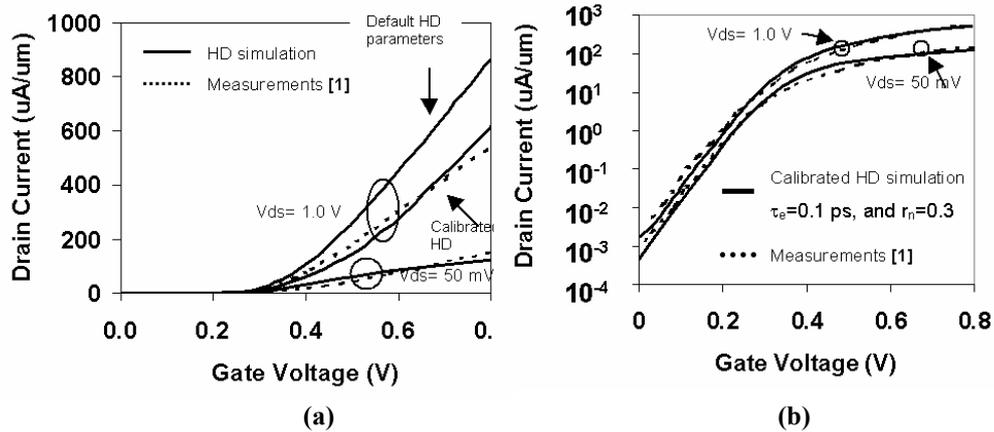


Figure 4: (a) Linear-scale plot of drain current vs. gate voltage for low ($V_{\text{ds}}=50$ mV) and high ($V_{\text{ds}}=1.0$ V) drain bias of the deeply scaled NWFET in [1] with the parameters in Fig.3. Shown is the measured data, uncalibrated HD (overestimates the current), and calibrated HD. A good fit is achieved using the Monte-Carlo bulk-Si HD parameters $\tau_e=0.1$ ps, and $r_n=0.3$. Using an “equivalent long-channel mobility” of 275 cm^2/Vs (constant as a function of gate voltage) captures the low drain bias I-V well.

(b) Logarithmic-scale plot of drain current vs. gate voltage for low ($V_{\text{ds}}=50$ mV) and high ($V_{\text{ds}}=1.0$ V) drain bias of the deeply scaled NWFET in [1] with the parameters in Fig.3. As can be seen the near ideal subthreshold swing (SS) and low DIBL are captured well. The density gradient model is used for quantization effects, which has efficient convergence with HD.