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Modeling NAND Flash Memories for Circuit Simulations

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Abstract

In this paper, we will present the basic structure and the parameter extraction procedure for a compact model of a NAND Flash memory string working in Spice-like circuit simulators. To the author knowledge, this is the first Spice-like model of a NAND Flash memory string. This model is modular and simple to be implemented. It will allow accurately reproducing both DC and transient behavior of NAND Flash memories without increasing computational effort, thus becoming an indispensable tool for designers to optimize circuits especially in multi-level applications.

1 Introduction

In the last years, the NAND Flash memory market has increased exponentially, mainly driven by digital camera memory card, MP3 player and USB card applications. Designing NAND Flash memories requires large use of Spice-like circuit simulations, which need accurate compact models to be effective [1]. Furthermore, an accurate NAND Flash compact model suitable for DC and transient simulations is strongly demanded for Multi-Level Cells (MLC) design, to optimize read algorithms and program/erase operations for present and future memory generations. In this scenario, we present in this paper the basic structure and the parameter extraction procedure for a compact model of a NAND Flash memory. The basic structure of the model is described in Section 2, whereas the parameter extraction procedure is illustrated in Section 3. Preliminary results are presented in Section 4. Conclusions follow.

2 Model structure

The basic structure of the compact model of a NAND Flash string is shown in Fig.1. This model is modular, and it is comprised of several circuit elements: two MOS transistors modeling Source Line (SL) and Bit Line (BL) selectors; *n* transistors connected in series, modeling the dummy cell, i.e. a Flash memory cell with Floating Gate (FG) and Control Gate (CG) short-circuited; the stacked ONO capacitors, C_{FC}; an array of capacitors accounting for the capacitive coupling to lateral and front/back cells. This model is physically based, thus allowing statistical and mismatch analysis,

and investigating process and technology variation effects. Since Spice-like simulators cannot solve a capacitive net in DC conditions [3], an internal procedure has been developed to calculate the Floating Gate (FG) potential. To achieve a higher accuracy [4] including also effects due to capacitive coupling to lateral and front/back cell Floating Gates [5], we extended the modeling approach proposed in [3]. Thus, the calculation of the FG voltage (V_{FG}) of the i-th cell comes from the solution of the charge balance equation.

$$\begin{aligned} &Q_G\left(V_{FG,i,j},V_{S,i,j},V_{D,i,j},V_{B,i,j}\right)+C_{FC}\left(V_{FG,i,j}-V_{CG,i,j}\right)+Q_{FG}+C_{FFB}\cdot \\ &\cdot\left(2V_{FG,i,j}-V_{FG,i-1,j}-V_{FG,i+1,j}\right)+C_{FL}\left(2V_{FG,i,j}-V_{FG,i,j-j}-V_{FG,i,j+1}\right)=0 \end{aligned} \tag{1}$$

Q_G is the charge on the MOSFET gate, whereas Q_{FG} is the program/erase charge on the FG. $V_{FG,i,j}$, $V_{S,i,j}$, $V_{B,i,j}$, and $V_{D,i,j}$ are FG, Source (S), Body (B) and Drain (D) voltages of the i-th cell in the j-th NAND Flash string, respectively. C_{FFB} and C_{FL} are the parasitic capacitances between adjacent cells in the same string and between cells belonging to adjacent strings, respectively. To account for program/erase, some current generators can be inserted between FG and S, B, and D to model tunneling currents flowing through the bottom oxide during program and erase operations [2].

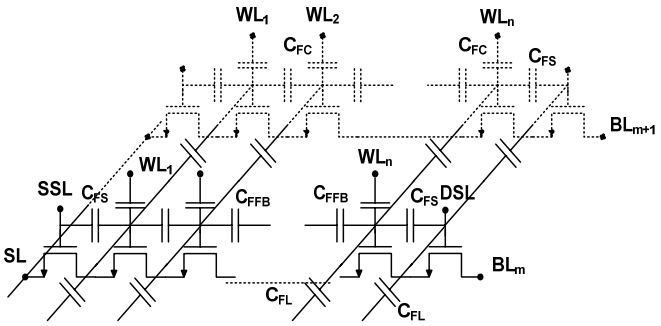

Figure 1: Schematic of basic structure of the NAND Flash string model.

3 Parameter extraction procedure

For the compact model to be effective and easy to be applied, a clear strategy should be developed to extract parameters of model elements: 1) the select transistor; 2) the equivalent dummy cell transistor; 3) the interpoly, front/back and lateral coupling capacitors. Since state-of-the-art NAND Flash technologies do not allow realizing single dummy cells because of manufacturing issues, we used a string of dummy cells to extract parameters of equivalent and select transistors in DC conditions. To this purpose, other devices in the dummy string are biased at a relatively high voltage to lower their channel resistance. Since some parameters (e.g. the length) of equivalent transistors depend on the position in the string, a *mean* model card has been extracted averaging model parameters extracted from measurements on 1st, 16th, and 32nd dummy cells, following the standard procedure adopted for BSIM4 transistor model.

A crucial problem that needs to be carefully taken into account for an accurate parameter extraction is the determination of the series resistance seen by the dummy cell which is to be extracted. The value of this resistance depends on the position of the cell inside the string, and it is due to channel and source/drain diffusion contributions. The source/drain diffusion resistance depends on the drain bias because of pronounced depletion effects. To account for these effects, non-linear resistance depending on drain and gate biases has been considered in series with the device to be extracted. The bias dependence of this resistance has been derived from both measures performed on a dedicated test structure of diffused resistors and TCAD simulations. The coupling capacitances (C_{FFL}, C_{FB}, C_{FS}) have been calculated by means of TCAD simulations and SEM measurements. To perform AC simulations allowing calculating coupling capacitances, we used the 3D structure of a small portion (3x3) of the NAND array, whose size and shape accurately resembles the cell characteristics derived from SEM measurements, not shown here for brevity.

4 Simulation results

Before verifying the simulation capability of the NAND Flash model, we checked the accuracy of the parameter extraction procedure of dummy cell and select transistors. Figure 2 shows I_D-V_G curves of the 16th dummy cell of the dummy string at different body voltages, while other dummy cells in the string are highly biased to lower their resistance. Spice-like simulations are performed adopting the average model card extracted considering the BSIM4 model. Measurements shown in Fig. 2, that refer to two corner case devices, have been obtained by measuring several NAND string in the whole array. As shown, simulations fall between the two corner I_D-V_G measurements for every V_B, demonstrating that the model extracted correctly describe the behavior of every equivalent transistor inside the NAND string. Similar results have been obtained also for the 1st and the 32nd dummy cells of the string and for the select transistor, not shown here for brevity. Then, we compared measurements performed on the string to simulations obtained with the compact model shown in Fig. 1. Figure 3 shows I_D-V_G trans-characteristics simulated and measured on the 16th cell of the string while applying a high gate voltage to the other cells. As shown, the agreement between simulations and measurements is excellent without any fitting parameter. This confirms the high accuracy of select and dummy transistor parameter extraction procedure and of TCAD simulations used to estimate coupling capacitance values. We obtained similar results also considering different cells in the string and different electrical curves, not shown here for brevity.

5 Conclusions

We proposed here a viable methodology for modeling a NAND Flash string, suitable for Spice-like circuit simulators. Following this methodology, we developed a compact model correctly reproducing the electrical behavior of a NAND Flash string without significantly increasing computation effort. In addition, the model is modular and very simple to implement, and it could be a valuable aid to design the next generation Multi-level NAND Flash memories.

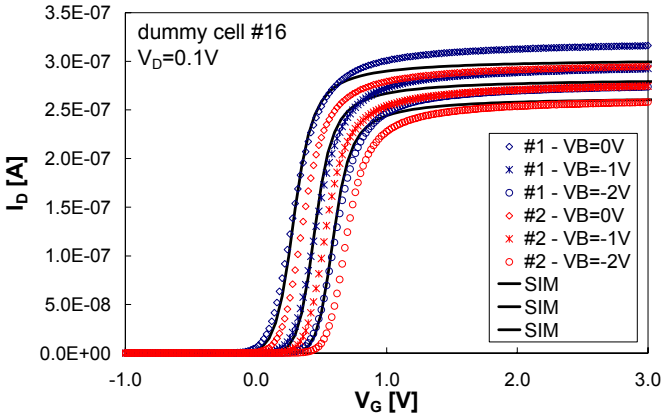

Figure 2: I_D-V_G curves simulated (solid lines) and measured (symbols) at different body biases (V_B) in the linear region (V_D=0.1V). The two sets of experimental data refer to two dummy cell corner cases.

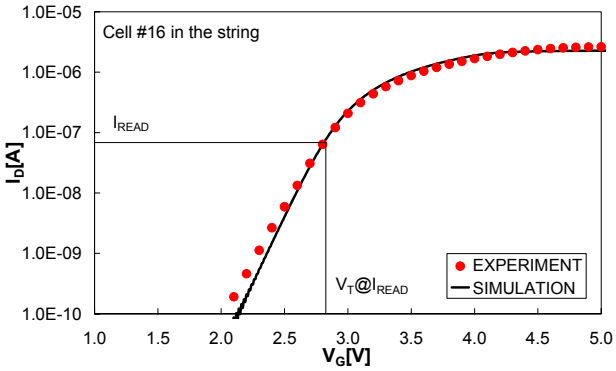

Figure 3: I_D-V_G curve simulated (solid lines) and measured (symbols) on the 16th cell in a string with V_B=0V and V_D=0.1V,

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