Compact Modeling for New Transistor Structures

C. Hu, M. Dunga, C-H. Lin, D. Lu, A. Niknejad

Department of EECS, University of California at Berkeley, CA 94720, USA

Abstract

Using embedded SRAM as a path, FinFET may enter manufacturing at 32nm. FinFET provides several advantages over the planar MOSFET structure----smaller size, larger current, smaller leakage, and less variation in threshold voltage. A compact model of multi-gate transistors will facilitate their adoption. BSIM-MG is a surface-potential based compact model of multi-gate MOSFETs fabricated on either SOI or bulk substrates. The effects of body doping are modeled. It can also model a double-gate transistor with independently biased front and back gates and asymmetric front and back gate work-functions and dielectric thicknesses.

1 Advantages of FinFET over Planar MOSFET

What makes a transistor different from a resistor is that the gate controls the conduction channel, not the drain. The gate exerts its control through capacitive (electrostatic) coupling to the channel. When we shrink the MOSFET gate to a smaller size, the drain is pulled closer to the (middle of the) channel. That increases the capacitive coupling between the drain and the channel. When the transistor is too small, the drain has enough coupling to the channel that a current (leakage current) flows with only a drain voltage applied without a gate voltage. This is the problem facing the planar transistor structure, which has not changed for four decades.

FinFET [1] allows the gate to control the channel from several sides (see Fig.1), thus increasing the gate control and allows the gate length to be reduced further. Since the introduction of FinFET, this structure has been used to set new world record of smallest gate length several times at various research laboratories. The current record is 3nm gate length. Clearly, FinFET can serve many technology nodes.

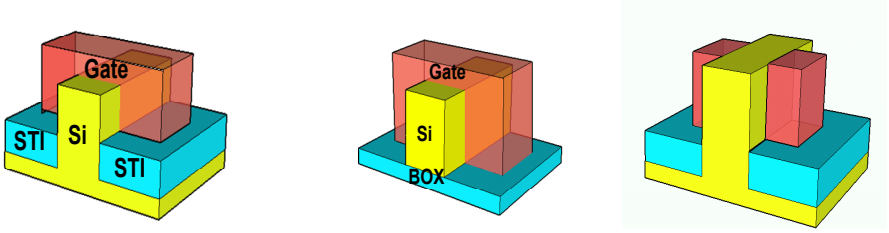

Fig. 1 (a) Bulk common-gate FinFET, (b) SOI common-gate FinFET, and (c) Bulk independent-gate FinFET.

FinFETs can coexist with planar MOSFETs in a conventional CMOS process with minimal additional process steps. By laying out two shallow-trench-isolations (STI) close together as shown in Fig. 1(a), we can create a silicon "fin" surrounded by STI oxide. The depth of the STI is around 200nm. Using one additional mask to recess the STI oxide by perhaps 40nm, we can expose a 40nm tall fin ready to be processed into a FinFET by going through the rest of the standard CMOS process flow. It is important to note that during the same process flow, conventional planar transistors can be also produced side by side on the same chip as the FinFETs. The fin height of the FinFETs is kept small and chosen to minimize the need for adjustments of the lithography, etching, and high-k dielectric deposition process modules.

Since FinFETs and planar transistors coexist, it is not necessary to replace the planar transistors in all the logic and analog circuits with FinFETs. We can, for example, use FinFETs in only the SRAM cells. Simulations have shown [2] that 45nm-node SRAM noise margin can be increased from 135mV to 175mV while the cell size is reduced by 20% when FinFETs replace the planar transistors. If an additional CMP process step is used to remove the top gate in Fig. 1(a) and turn the structure into Fig. 1(c), each fin now has two gates that are electrically independent. In that case, the noise margin improved further to 300mV. These simulations were conducted with a mixed-mode device-circuit simulator. A compact model for these new transistor structures would allow much faster circuit research and design using SPICE circuit simulators.

2. A Modular and Versatile Compact Model

The versatility of the BSIM-MG model is achieved without sacrificing its computational efficiency. One technique used is to introduce dual modules. BSIM-CMG is a common-gate module and BSIM-IMG is an asymmetric/independent-gate module. "Common-gate" means that there is only one electrically interconnected gate (one gate voltage) whether the device structure is a double, triple, or quadruple gate structure. Examples are Fig. 1(a) and (b). The common-gate module assumes that the gate work-functions and the dielectric thickness on the two, three, or four active sides of the fin are the same. The carrier mobility on the vertical and horizontal channels may be different because of the different crystal orientations and/or strain.

The asymmetric/independent-gate module allows the front and back gate work-functions and dielectrics to be different. It assumes that the two gates have different voltages in general. The bottom gate can be used, for example, to adjust the threshold voltage of the top channel.

3 The Model

Previous analytical DG-MOSFET core models ignored the body doing [3,4,5]. BSIM-CMG includes body doping because body doping is needed to support multi-Vt technologies. The Poisson's equation is perturbed by the body doping such that a

modification term to the surface potential is derived. The analytical surface potential agrees well with TCAD double-gate device simulation for different fin doping concentrations without any fitting parameters (Fig. 2).

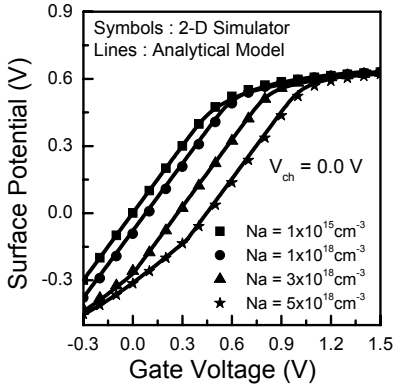

Fig. 2 Surface potential model agrees with TCAD simulation results well without any fitting parameters in both partially depleted and fully depleted regimes and for both lightly doped and heavily doped DG-MOSFETs.

Drift-diffusion equation [6] is then employed to obtain the drain current in terms of the surface potentials at the source and the drain. The I-V core model predicts drain current accurately in all regimes of operation without any fitting parameters. Volume inversion is correctly modeled in the solution of the Poisson's equation and the I-V formulation (Fig. 3).

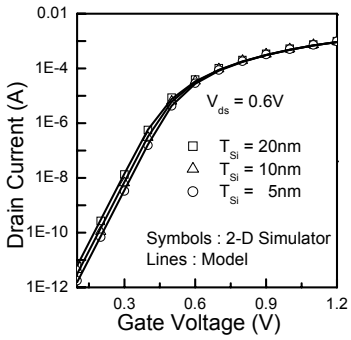

Fig. 3 I-V core model accurately predicts drain current for different body thickness, *Tsi*. Volume inversion is captured---the subthreshold current is proportional to the body thickness.

Furthermore, a separate core model has been developed for the asymmetric/independent-gate MOSFETs. It also has excellent accuracy. The threshold voltage tuning by the back gate bias is accurately predicted by the model.

To model the short cahnnel effect, Poisson's equation is solved for the minimum potential barrier in the body [7,8]. A lower gate voltage is needed to obtain the same

threshold barrier potential for a short channel device than the core model thus necessitating a V_g modification term. Gate leakage is of course also modeled as are the quantum mechanical effects on current and capacitance. BSIM-MG also supports FinFETs fabricated on SOI and those fabricated on bulk substrates.

4 Verification with Experimental Data

The model is verified against two different FinFET technologies – SOI FinFETs and bulk FinFETs [9]. BSIM-MG was able to describe the trends in I_d and its derivatives for both technologies as shown in Fig. 4.

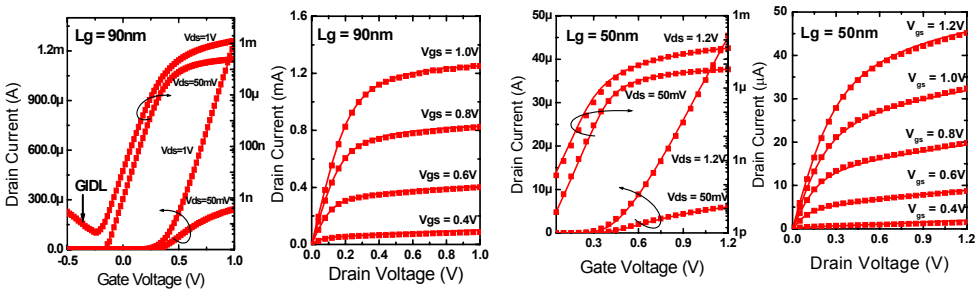

Fig. 4 Verification of the model (lines) with measured data (points) of FinFETs on SOI substrates (two figures on the left) and bulk substrates (two figures on the right).

Acknowledgements

This research is sponsored by SRC and MICRO. Data in Fig. 4 are supplied by TI and TSMC.

References

[1] X. Huang et al.,"Sub-50 nm FinFET: PMOS", 1999 IEDM, p.67.
[2] Z. Guo et al., "FinFET-based SRAM design," *International Symp. Low Power Electronics and Design*, August 2005.
[3] Y. Taur, IEEE TED, vol. 48, pp. 2861-2869, 2001
[4] D. Jiminez et al., JAP, vol. 94, pp. 1061-1068, 2003
[5] *G.D.J. Smit*, et al., "PSP-based compact FinFET model describing dc and RF measurements ", *IEDM Tech. Dig., p.175, 2006*
[6] J. R. Brews, SSE, vol. 21, pp. 345-355, 1978
[7] K. Suzuki el al., IEEE TED, vol. 40, pp. 2326-2329, 1993
[8] R. Yan et al., IEEE TED, vol. 39, pp. 1704-1710, 1992
[9] M. Dunga et al., "BSIM-MG: A Versatile Multi-Gate FET Model for Mixed-Signal Design", 2007 VLSI Technology Symposium.