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Electrothermal Monte Carlo Study of Charge Confinement in GaN HFETs

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Abstract

An electrothermal Monte Carlo method is applied to study various GaN heterostructures designed to improve electron confinement in the channel of the structures. It is shown that the use of a p-type GaN buffer and the inclusion of a thin InGaN back-barrier below the channel in AlGaN/GaN HFETs improve the device pinch-off characteristics, but increase the influence of self-heating. Results show that the use of an AlGaN exclusion layer at the AlGaN/GaN interface increases both the device currents and temperatures.

1 Introduction

The reduction in the gate lengths of heterostructure field-effect transistors (HFETs), to provide higher operation frequencies, is accompanied by an increase in the importance of short-channel effects, as the use of short gate lengths weakens the dependence of the device characteristics on the gate bias [1]. Such effects can be minimised by the improvement of electron confinement in the channel. This work is a comparison of electron transport, simulated using an electrothermal Monte Carlo (MC) method, in various GaN HFETs designed to improve charge confinement in the channel.

2 Simulation Method, Results and Discussions

This work was carried out using an electrothermal simulator, iteratively coupling a two-dimensional (2-D) MC method with a three-dimensional solution of the heat diffusion equation. The coupling approach for a simple 2-D electrothermal model is described in [2]. Results are generated for an $Al_{0.15}Ga_{0.85}N$/GaN HFET with an n-type buffer (structure I) shown in Fig. 1, and three other structures similar to structure I but with additional features, including an $Al_{0.15}Ga_{0.85}N$/GaN HFET with a p-type buffer of concentration $4 \times 10^{22}\,m^{-3}$ (structure II), an $Al_{0.15}Ga_{0.85}N/GaN/In_{0.15}Ga_{0.85}N$/GaN HFET with a 2 nm $In_{0.15}Ga_{0.85}N$ (back-barrier) layer inserted at the bottom of the channel (structure III) and an $Al_{0.15}Ga_{0.85}N/Al_{0.5}Ga_{0.5}N/GaN/In_{0.15}Ga_{0.85}N$/GaN HFET with a 2 nm $Al_{0.5}Ga_{0.5}N$ exclusion layer inserted between the spacer and the channel and a 2 nm $In_{0.15}Ga_{0.85}N$ layer inserted below the channel (structure IV). All the structures are assumed to include a 1μm GaN buffer layer built on a 6H-SiC substrate. The die width is 500μm and the die length and depth are 100μm. The gate width is 100μm. We apply the same thermal boundary conditions described in [2] at the die surfaces.

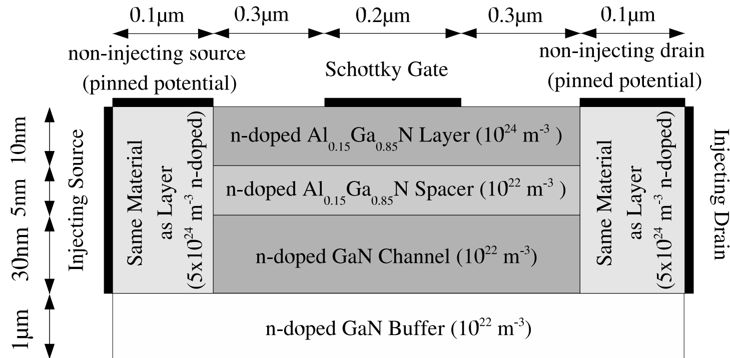

Figure 1: The electronically simulated region of the basic single heterojunction $Al_{0.15}Ga_{0.85}N$/GaN HFET (structure I). The 2 nm $In_{0.15}Ga_{0.85}N$ back-barrier (in structures III and IV) and the 2 nm $Al_{0.15}Ga_{0.85}N$ exclusion layer (in structure IV) are n-doped with a concentration of $10^{22}\,m^{-3}$. The Schottky barrier is 1.5 eV.

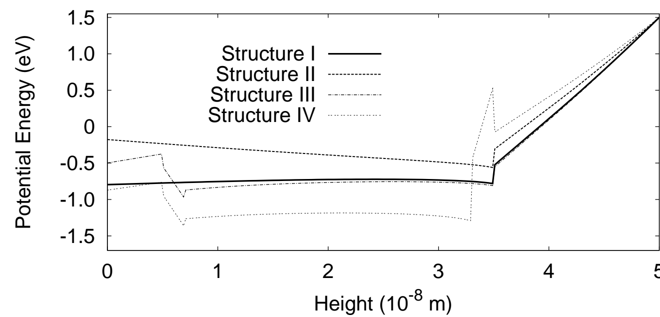

Figure 2: Time-averaged conduction band edge for the central valley, under the centre of the gate, for $V_{gs} = 0$V and $V_{ds} = 7.0$V. The device top surface is at $y = 5 \times 10^{-8}$ m.

In structures II and III, the number of electrons flowing into the GaN buffer is reduced. This reduction is achieved in structure II by raising the conduction band in the buffer with respect to the channel and in structure III by creating an effective potential barrier below the channel, as demonstrated in Fig. 2, which shows profiles of the conduction band edge for the central Γ_1 valley. In structure IV, the high potential barrier created at the $Al_{0.5}Ga_{0.5}N$/GaN interface prevents electrons from moving to the top AlGaN layers, which minimises the effect of impurity and alloy disorder scattering on the device performance. From the transfer characteristics shown in Fig. 3, structures II and III demonstrate excellent pinch-off characteristics, due to the improvement of carrier confinement in the channel. Although the current handling capability of structure III is not seriously affected, that of structure II is reduced. The current handling capability of structure IV is improved due to the lowering of the conduction band in the channel with respect to the Schottky gate (see Fig. 2) resulting in higher electron concentrations. Fig. 4 shows the variation of the ratio of the average x component of the current den-

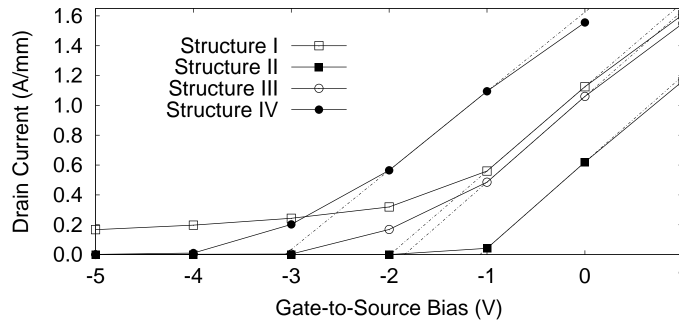

Figure 3: Transfer characteristics of the structures at a 10.0 V drain-to-source bias. The pinch-off voltage V_p is determined by defining the gate-to-source bias intercept of the extrapolation of the drain current at the point of peak transconductance. V_p is approximately -2.0 V, -1.0 V, -2.0 V and -3.0 V for structures I, II, III and IV, respectively.

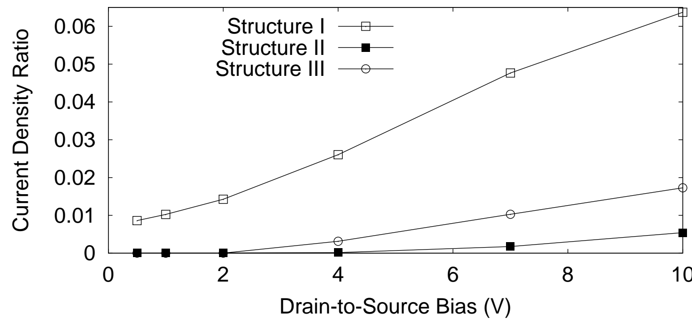

Figure 4: Variation of the ratio of the average x component of the current density in the buffer to that in the channel with V_{ds}, at $(V_{gs} - V_p) = 2.0$V, for structures I, II and III.

sity in the buffer to the average x component of the current density in the channel, for structures I, II and III, at the same $(V_{gs} - V_p)$ (V_{gs} is the gate-to-source bias and V_p is the pinch-off voltage). The lowest ratio values in structure II suggest that this structure provides more effective charge confinement than structure III. Fig. 5 shows the peak temperature variation with the total macroscopic power dissipation in the simulated structures. While structures II, III and IV all enhance self-heating effects, structure II has the highest device temperatures. Fig. 6 shows the variation of the electron density along the y-axis, for the four structures at the same $(V_{gs} - V_p)$ and drain-to-source bias (V_{ds}), at the location of the peak mean electron energy in the x-axis. The importance of self-heating in structures II, III and IV (demonstrated in Fig. 5) can be explained by the increase in the number of highly-energetic electrons in the channel (due to better confinement), in areas characterised by non-equilibrium transport, resulting in higher power densities and peak temperatures. Structures II and III suffer from the disadvantage of increasing the number of electrons leaving the channel to the top AlGaN layers, an effect significantly minimised when using an AlGaN exclusion layer.

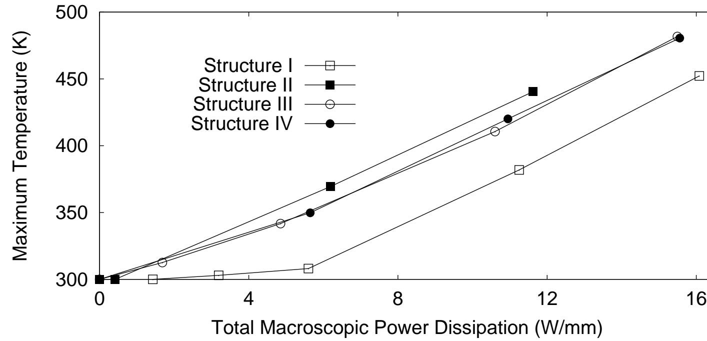

Figure 5: Peak temperature variation with the macroscopic power dissipation for the structures, at a 10.0 V drain-to-source bias, for a range of gate-to-source biases.

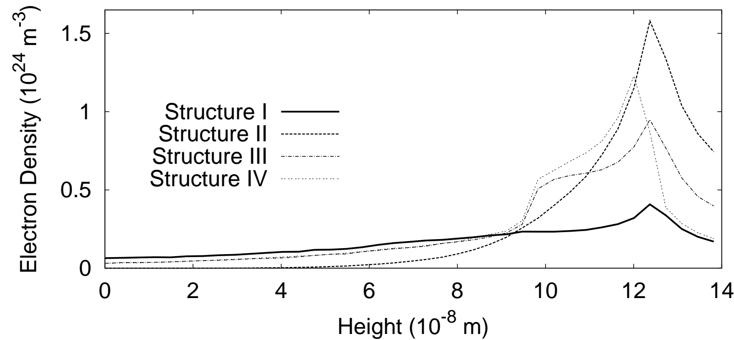

Figure 6: Electron density variation along the y-axis, at $(V_{gs} - V_p) = 2.0$V and $V_{ds} = 10.0$V, at the peak mean electron energy location in the x-axis (at $x = 6.35 \times 10^{-7}$ m, where the start of the source region is at $x = 0$). The top surface is at $y = 14 \times 10^{-8}$ m.

3 Conclusions

Electron transport is studied in GaN HFETs designed to improve charge confinement, using an electrothermal MC simulator. It is shown that the use of a p-type buffer and an InGaN back-barrier provide better pinch-off characteristics but also increase the importance of thermal effects. It is shown that structures incorporating an AlGaN exclusion layer are characterised by higher current handling capabilities and device temperatures.

References

[1] M. J. Uren, K. J. Nash, R. S. Balmer, T. Martin, E. Morvan, N. Caillas, S. L. Delage, D. Ducatteau, B. Grimbert and J. C. De Jaeger, "Punch-Through in Short-Channel AlGaN/GaN HFETs", IEEE Trans. Electron Devices, vol. 53, pp. 395398, 2006.

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