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Simulation of Lag and Current Slump in AlGaN/GaN HEMTs as Affected by Buffer Trapping

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Abstract

Two-dimensional transient simulations of AlGaN/GaN HEMTs are performed in which a deep donor and a deep acceptor are considered in a semi-insulating buffer layer. It is shown that lag phenomena and current slump could be reproduced. Particularly, it is shown that gate lag is correlated with relatively high source access resistance of AlGaN/GaN HEMTs, and that drain lag could be a major cause of current slump. The current slump is more pronounced when the deep-acceptor density in the buffer layer is higher and when an off-state drain voltage is higher, because trapping effects become more significant. It is concluded that an acceptor density in the buffer layer should be made low to minimize current slump, although current cutoff behavior may be degraded when the gate length is short.

1 Introduction

Recently, AlGaN/GaN HEMTs have received great attention because of their potential applications to high power microwave devices [1]. However, slow current transients are often observed even if the drain voltage V_D or gate voltage V_G is changed abruptly (called drain lag or gate lag) [2]. The slow transients mean that dc *I-V* curves and RF *I-V* curves become quite different, resulting in lower RF power available than that expected from dc operation [1,2]. This is called power slump or current slump. These are serious problems, and there are many experimental works reported [1-5]. However, only a few theoretical works are made recently[4,6], where effects of a donor-type surface state (near the valence band) or effects of a bulk deep acceptor (~ 1 eV above the midgap of GaN) are studied for gate lag or pulsed *I-V* curves in AlGaN/GaN HEMTs. But, the type of traps and their energy levels seemed to be artificial. So, in this work, we have made simulations of AlGaN/GaN HEMTs with a semi-insulating buffer layer in which trap levels based on experiments are considered, as in our previous work on GaN MESFETs [7], and showed that the lag phenomena and current slump could be reproduced. Particularly, we show that the gate lag is correlated with relatively high source access resistance of AlGaN/GaN HEMTs, and also give a way to reduce the current slump.

2 Physical Model

Fig.1 shows an analyzed AlGaN/GaN HEMT structure. As a model for the semi-insulating buffer layer, we use a three-level compensation model which includes a

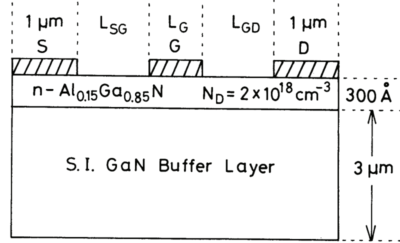

Figure 1: Modeled AlGaN/GaN HEMT analyzed in this study.

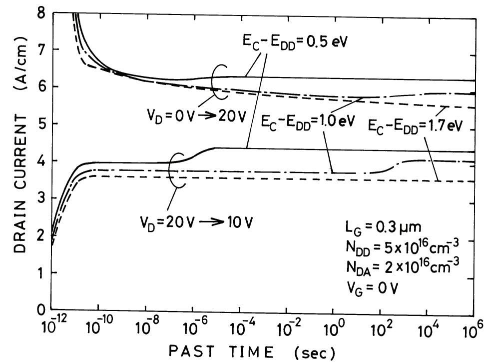

Figure 2: Calculated drain-current responses as a parameter of E_{DD} when V_D is raised abruptly from 0 V to 20 V (upper) or when V_D is lowered abruptly from 20 V to 10 V (lower). $V_G = 0$ V.

shallow donor, a deep donor and a deep acceptor. Some experiments show that two levels (E_C – 1.7 eV, E_C – 2.85 eV) are associated with current slump in GaN-based FETs [2], so that we use energy levels of E_C – 2.85 eV (or E_V + 0.6 eV) for the deep acceptor and of E_C – 1.7 eV for the deep donor. Other experiments show shallower energy levels for deep donors in GaN [8], and hence we vary the deep donor's energy level E_{DD} as a parameter. Basic equations are Poisson's equation including ionized deep-level terms, continuity equations for electrons and holes which include carrier loss rates via the deep levels, and rate equations for the deep levels. We have calculated the drain current responses when V_D and/or V_G are changed abruptly.

3 Lag Phenomena

Fig.2 shows calculated responses of drain current I_D when V_D is raised or lowered abruptly, where V_G is kept constant. When V_D is raised, I_D overshoots the steady-state value, because electrons are injected into the buffer layer, and deep traps there need certain time to capture these electrons. On the other hand, when V_D is lowered, I_D remains at a low value for some periods and begins to increase slowly, showing drain lag behavior. It is understood that the drain currents begin to increase as the deep donors begin to emit electrons. These drain lags are also reported experimentally in AlGaN/GaN HEMTs [2,5].

We have next calculated a case when V_G is also changed. Fig.3 shows calculated turn-on characteristics when V_G is changed from the threshold voltage V_{th} to 0 V, with on-state drain voltage V_{Don} as a parameter. The characteristics are similar to those in Fig.2, and hence the change of V_D (drain lag) is regarded as essential in this case. However, as seen in the uppermost curve of Fig.3, some transients are observed when only V_G is changed. This indicates that gate lag occurs due to deep levels in the buffer layer. We will describe below why the gate lag arises. Fig.4 shows a comparison of (a) conduction-band-edge energy profiles, (b) electron density profiles, and (c) ionized-deep donor density N_{DD}^+ profiles between the off state and the on state. Note that only V_G is different here. From Fig.4(a), in the on state, some potential drops are

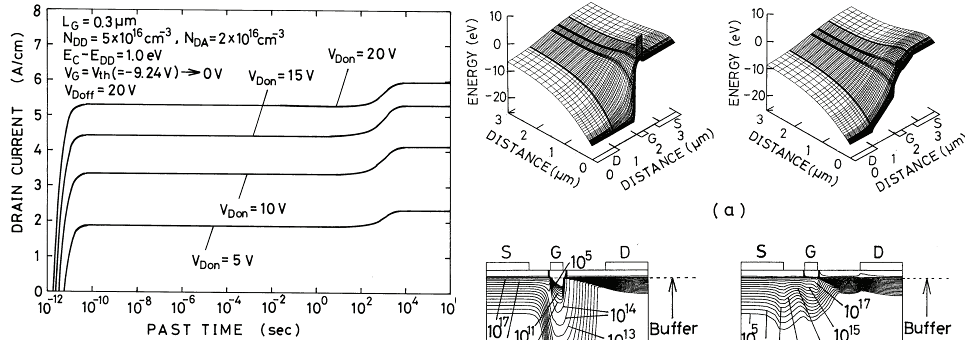

Figure 3: Calculated turn-on characteristics when V_G is changed from threshold voltage V_{th} to 0 V, with on-state drain voltage V_{Don} as a parameter. Off-state drain voltage V_{Doff} = 20 V. $E_C - E_{DD}$ = 1.0 eV.

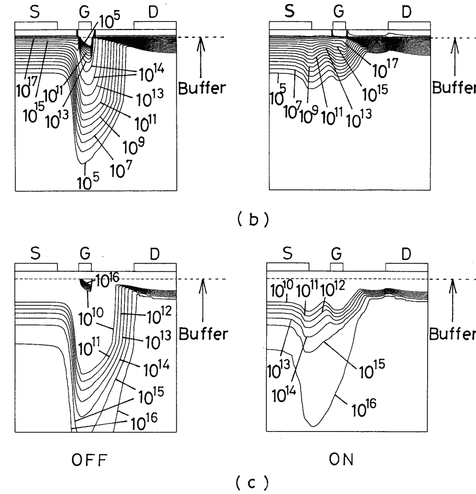

Figure 4: (a) Conduction-band-edge energy profiles, (b) electron density profiles, and (c) ionized deep-donor density N_{DD}^+ profiles when only V_G is different. The left is for $V_G = V_{th} = -9.24$ V and V_D = 20 V (OFF), and the right is for V_G = 0 V and V_D = 20 V (ON).

observed between source and gate, indicating that source access resistance becomes important. It is understood that due to this potential drop at the source side, when V_G becomes negative and the channel is depleted, electrons do not all flow into the source and drain electrodes, but can be injected into the buffer layer as seen in Fig.4(b). These electrons are captured by deep donors, and hence N_{DD}^+ decreases in the off state, as seen in Fig.4(c). Because of this increase in negative space charges in the buffer layer, even if V_G is switched on, I_D remains at a low value until the deep donors begin to emit electrons, showing gate-lag behavior.

4 Current Slump

Next, we have studied dependence of current slump on deep-level densities in the buffer layer. Fig.5 shows calculated I_D-V_D curves for different deep-acceptor density N_{DA}. In this figure, we plot by point (x) the drain current at $t = 10^{-8}$ s after V_G is switched on. This is obtained from the turn-on characteristics, and this curve corresponds to a quasi-pulsed I-V curve with pulse width of 10^{-8} s. It is seen the drain currents in the pulsed I-V curves become rather lower than those in the steady state, showing current slump behavior. This type of current reduction is commonly observed experimentally in AlGaN/GaN HEMTs. It is clearly seen that the current slump is more pronounced for higher N_{DA}. This is because trapping effects become more remarkable due to higher ionized (empty) deep-donor density N_{DD}^+. It is concluded that the acceptor density must be made low to minimize current slump.

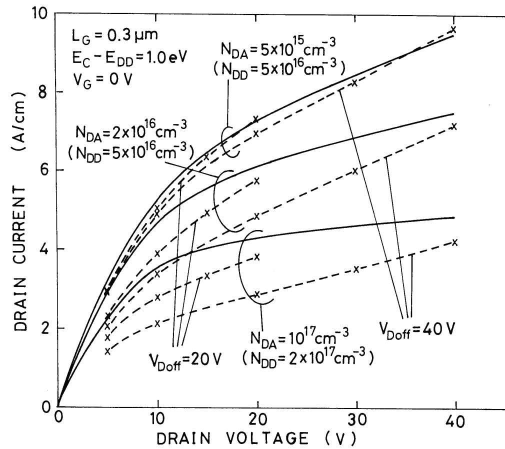

Figure 5: Steady-state *I-V* curves (V_G = 0 V; solid lines) and quasi-pulsed *I-V* curves (x; $t = 10^{-8}$ s) from off points for AlGaN/GaN HEMTs with different N_{DA}. $E_C - E_{DD}$ = 1.0 eV.

Finally, we have studied dependence of current slump on an off-state drain voltage V_{Doff}. As seen in Fig.5, the current slump is more pronounced for higher V_{Doff}, and contribution of drain lag to it becomes large. This is because for higher V_D, electrons are injected deeper into the buffer layer and more electrons are captured by the deep donors, resulting in heavier current reduction. This tendency is also reported experimentally in AlGaN/GaN HEMTs [3].

5 Conclusion

Two-dimensional transient simulations of AlGaN/GaN HEMTs have been made in which a three-level compensation model is adopted for the buffer layer. The lag phenomena and current slump could be reproduced. Particularly, it has been shown that the gate lag is correlated with relatively high source access resistance of AlGaN/GaN HEMTs, and that the drain lag could be a major cause of current slump. It is concluded that an acceptor density in the buffer layer should be made low to minimize current slump, although current cutoff behavior may be degraded when the gate length is short.

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