Transport in Silicon Nanowire and Single-Electron Transistors

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Abstract

We have extensively investigated transport properties of nanowire MOSFETs and single-electron/single-hole transistors by experiments and band calculations. Special focus has been placed on measurements and physics of the channel direction dependence and charge polarity dependence. We adopted a special device structure with a common n-type and p-type channel. We confirmed that a [110]-directed nanowire p-type FET has the smallest V_{th} fluctuations caused by the size variations. We also verified that a [100]-directed single-hole transistor is the best device for the single-charge transistor operations. Actually, we observed Coulomb blockade oscillations with the record high peak-to-valley-current ratio of 480 at room temperature in a [100] single-hole transistor.

1 Introduction

A nanowire MOSFET is one of the most promising devices in terms of short channel immunity by better gate controllability and possible high performance operation due to ballistic transport [1-6]. In a nanowire FET, device characteristics are largely affected by the two-dimensional quantum confinement of carriers in a nanowire channel [1-2]. Therefore, the fundamental understanding of physics and modeling are essential for future developments of nanowire FETs. However, only a few experimental works have been reported previously on the quantum confinements in nanowire FETs, and qualitative and quantitative comparison between experimental data and simulation/modeling have not been sufficient.

On the other hand, silicon nanowire structure is also suitable for a single-electron transistor (SET) and a single-hole transistor (SHT) operating at room temperature [7-9]. SETs and SHTs have high functionalities with ultra low power dissipation, which cannot be attained by the conventional CMOS scheme. In an extremely narrow nanowire channel, tunneling barriers and an ultrasmall silicon dot are self-formed due to local large quantum confinement and the nanowire FET operates as a single-electron/hole transistor. However, the influence of channel structure on SET/SHT characteristics and the channel direction dependence still remain unclear.

In this study, we extensively investigate the transport properties of nanowire FETs and SETs/SHT at room temperature. Special emphasis is placed on the channel direction dependence and charge polarity dependence. We fabricate [100]- and [110]-directed nanowire NFET and PFET as well as SET and SHT, and their transport is measured intensively at room temperature. The channel direction and charge polarity dependences in nanowire FET and SET/SHT are clarified.

2 Device Structure and Fabrication

Figure 1 (a) shows a schematic of a nanowire FET and SET/SHT measured in this study. The device has a special feature: the device has both n-type source/drain and p-type source/drain that are connected to the nanowire channel [2, 10]. The device acts as an NFET when a positive voltage is applied to the gate, while the device acts as a PFET when a negative voltage is applied to the gate. Thanks to this special structure, transport properties of both electron and hole can be studied in the entirely same physical channel profile.

SOI thickness of the nanowire channel is finally reduced to 3-4 nm by SC1 wet etching and thermal oxidation. The thickness of gate oxide is 10nm. The channel width is designed ranging from almost 0 nm to 18 nm. Figure 1 (b) shows the configuration of nanowire FETs. Silicon nanowire channels are directed to [100] and [110] on (100) SOI substrate. In [100]- and [110]-directed nanowires, the side wall surfaces are oriented to (010) and (110), respectively.

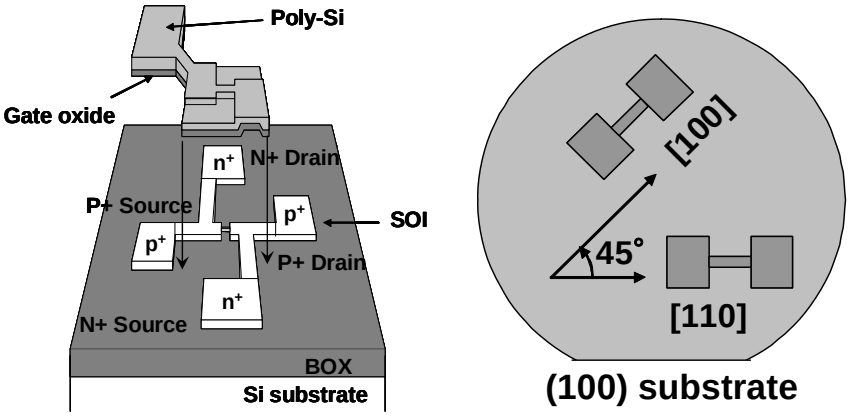

Figure 1: (a) A schematic of the special device structure adopted in this study. (b) A schematic of channel direction on a (100) substrate.

3 Quantum Confinement Effects in nanowire FETs

Figures 2 shows drain current (I_d) versus gate voltage (V_g) characteristics of [100]- and [110]-directed nanowire FETs with channel width designed from 2nm to 18nm. In [100] nanowire FETs, the threshold voltage variations (ΔV_{th}) is larger in PFET than in NFET, and in [110] nanowire FETs, ΔV_{th} is larger in NFET than in PFET. Figure 3 shows the ΔV_{th} plots for NFET versus PFET. From this figure, while ΔV_{th} in NFET is almost the same, ΔV_{th} in [110] PFET is significantly small compared to [100] PFET. The origin of the V_{th} variations is the quantum confinement effects in nanowire channel. When the channel width fluctuates, the degree of the quantum confinement effects varies, resulting in the V_{th} fluctuations. The measured dependence on the channel directions and charge polarity can be explained by the subband structure in nanowire channels.

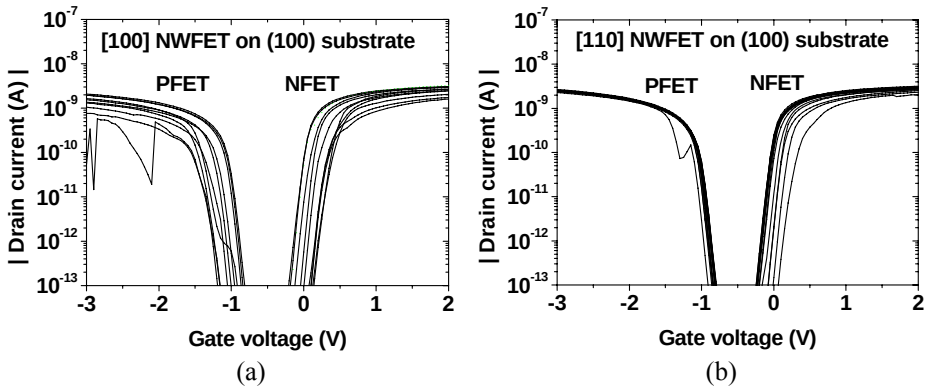

Figure 2: Measured I_d - V_g characteristics in (a) [100]-directed nanowire FETs and (b) [110]-directed nanowire FETs.

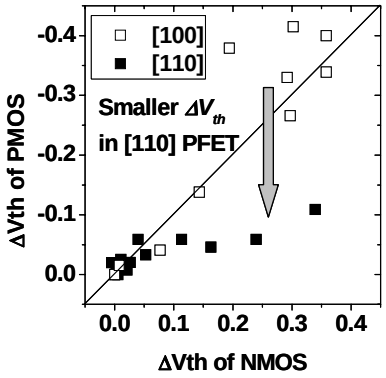

Figure 3: Measured ΔV_{th} in PFET vs, ΔV_{th} in NFET in [100]- and [110]-directed nanowire FETs.

In order to examine quantum confinement in both channel directions, we calculated the subband energy in silicon nanowire channels. The effective mass method is adopted for conduction band, and the Luttinger Hamiltonian method is adopted for valence band. Figure 4 shows the subband energy in conduction band and valence band as a function of channel width. In [110] channel, the subband energy is larger in NFET than in PFET. In [100] channel, the subband energy is larger in PFET than in NFET. Especially in PFET, the subband energy is smaller in [110] than in [100]. A [110] PFET has the smallest subband energy, and therefore, these calculation results agree with the experimental ΔV_{th} result. The [110] nanowire NFET and PFET are expected to have high performance in terms of I_{on} [5]. This small V_{th} fluctuations support the superiority of [110] nanowire PFET.

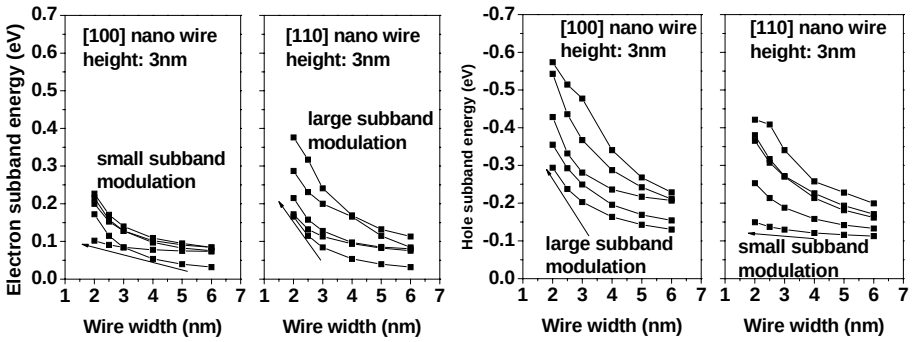

Figure 4: Calculated subband energy in (a) conduction band and (b) valence band in [100]-directed nanowire and [110]-directed nanowire.

4 Quantum Confinement Effects in SETs and SHTs

Figure 5 shows I_d - V_g characteristics of [100] and [110] SETs and SHTs at room temperature. Clear Coulomb blockade oscillations are observed, and the characteristics and peak-to-valley-current ratio (PVCR) vary depending on the charge polarity (electron or hole) and channel directions. Figure 6(a) compares measured PVCR of the Coulomb blockade oscillations in SETs and SHTs. Large PVCR indicates large additional energy which consists of classical charging energy and quantum level spacing in silicon quantum dot [11]. Deviation from the center solid line means the difference of quantum confinement between SET and SHT. In [100] channel, PVCR of SHT is much larger than that of SET. In [110] channel, PVCR of SET is larger than that of SHT.

Figure 6(b) shows comparison of peak current (I_{peak}) of Coulomb blockade oscillations in SHT and SET. I_{peak} indicates the tunneling barrier height. Small I_{peak} means high tunneling barrier. In [110] channel, I_{peak} of SET is smaller than that of SHT. In [100] channel, I_{peak} of SHT is smaller than that of SET.

These channel direction dependence of SETs and SHTs can be also explained by the nanowire subband structure in the same way as nanowire FETs. Large subband energy induced by local large quantum confinement leads to higher tunneling barriers and a silicon quantum dot sandwiched by large tunneling barriers has large quantum level spacing.

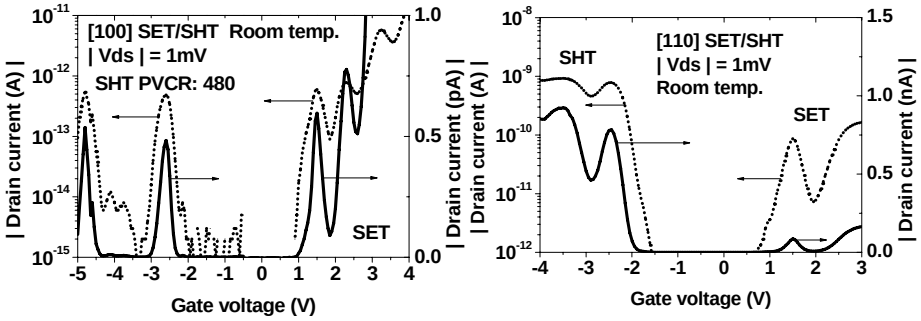

Figure 5: Measured characteristics in (a) [100]-directed SETs and SHTs and (b) [110]-directed SETs and SHTs at room temperature.

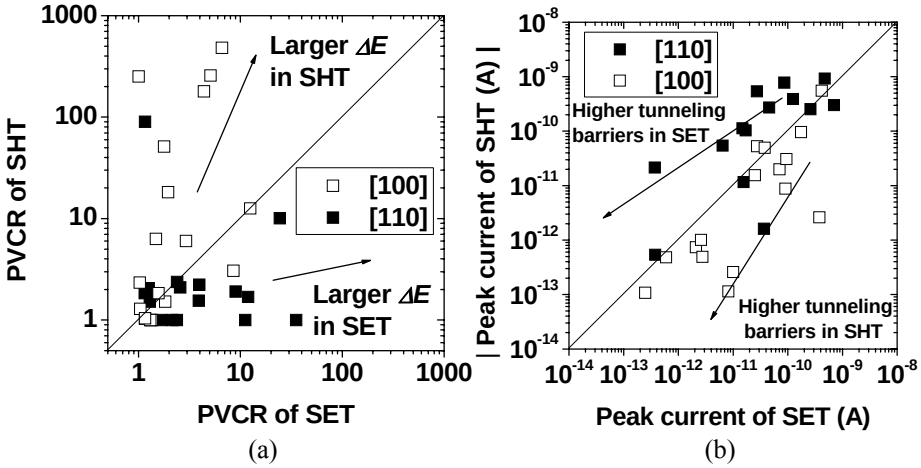

Figure 6: Measured data of (a) comparison between PVCR in SHT vs. PVCR in SET and (b) comparison between peak current of SHT vs. peak current of SET at room temperature.

From these results, the most optimized structure in terms of large PVCR of the Coulomb blockade oscillations is a [100]-directed SHT. Figure 7(a) shows the largest Coulomb blockade oscillations ever reported in a [100]-directed SHT at room temperature. PVCR is as high as 480. Figure 7(b) shows measured I_d of the same SHT as a function of drain voltage, instead of gate voltage, at room temperature. Clear negative differential conductance (NDC) is observed due to large quantum level spacing in a dot. PVCR of NDC of 300 is the highest ever reported in a SET/SHT system. Analog/digital high functional circuits can be achieved by these clear Coulomb blockade oscillations [8] and NDC [7].

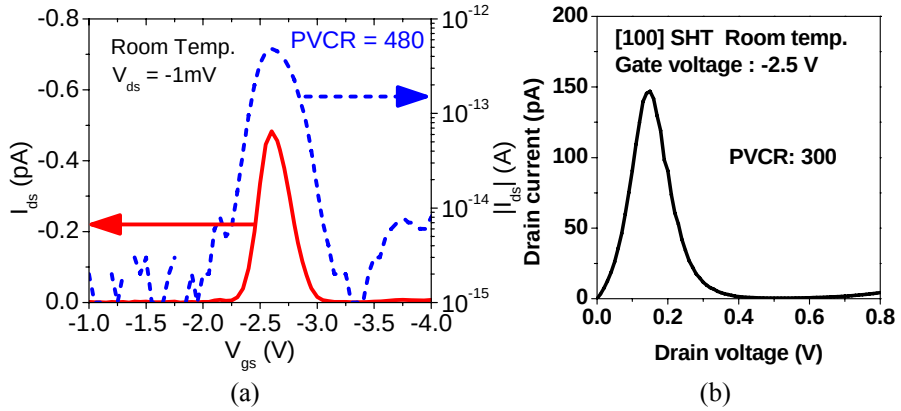

Figure 7: Measured characteristics of (a) Coulomb blockade oscillations and (b) negative differential conductance in a [100]-directed SHT at room temperature.

5 Conclusion

The transport properties of silicon nanowire FETs and single-electron/hole transistors are intensively investigated. The transport of nanowire FETs and SET/SHT is largely affected by the quantum confinement effects in a nanowire channel and a dot. It is found that a [110]-directed nanowire PFET has smallest V_{th} fluctuations due to small subband energy in the nanowire channel. It is also found that a [100]-directed SHT is the best single-charge device in terms of large Coulomb blockade oscillations due to the largest subband energy in the nanowire and the dot.

Acknowledgements

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