# Study of Time-Periodic Avalanche Breakdown Occurring in VLD Edge Termination Structures

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#### Abstract

IGBT device destruction often occurs localized at the edge termination. Among various termination techniques, "variation of lateral doping" (VLD) is a promising candidate to increase the ruggedness of IGBT chips. We analyzed the time-dependent behavior of VLD edge termination during avalanche breakdown by numerical simulations demonstrating the advantage of this technique. Measurements on IGBT test devices with VLD edge termination are in agreement with the simulations.

#### **1** Introduction

Achieving the largest possible safe-operating area is a major concern in industrial applications. The safe-operating area of power devices is determined by the maximum voltage and current within which the device operates without failure. The devices considered here are arrays consisting of many thousands of parallel IGBT cells, which are encompassed by an edge termination structure to attain the maximum breakdown voltage. IGBT cell arrays, in contrast to certain DMOS transistor cell arrays [1], tend to break down at their periphery. "Variation of lateral doping" (VLD) is a promising edge termination technique to enhance the ruggedness of IGBT cell arrays and, at the same time, to reduce the size of the termination structure on the die.

### 2 Simulation

We studied the time-dependent internal device behavior in the vicinity of the VLD edge termination (Fig. 1) during avalanche breakdown using the device simulator DESSIS [2]. The device region considered (Fig. 1) is a cylindrical ring with the radius of curvature chosen in accordance with the real structure; it represents one of the four corners of the IGBT cell array, which constitute the weakest parts of the cell array as confirmed by infrared photoemission detection in the blocking state. In order to speed up the simulations the structure is, in a first step, isothermally driven towards avalanche breakdown by applying a quasistationary voltage-ramp. This is followed by an electro-thermally coupled transient simulation with an ideal heat sink at the backside of the device, while the voltage ramp is continued above the breakdown voltage and, then, kept constant for approximately 100 µs.

Fig. 2 shows the time-dependent current that flows through the VLD structure while a constant voltage is applied. As most striking feature, we find a periodic sequence of sharp current peaks (cf. Fig. 3), the period of which decreases with increasing voltage (cf. Fig. 2). The current peaks are caused by periodically evolving, moving and finally self-extinguishing current filaments, which are generated by avalanche multiplication occurring at the bending of the p-body, then move away from the self-heated point of origin and, finally, vanish at the left border of the simulation region (cf. Fig. 4, Fig. 5 and Fig. 6 for the current distribution and the temperature distribution, respectively, at different times). The increase of the peak frequency with increasing voltage can be



Figure 1: Simplified schematic structure of the edge termination investigated. "Variation of lateral doping" (VLD) is a p-doped region, with gradually decreasing doping towards the right border.



Figure 2: Periodic current peaks as observed under avalanche breakdown conditions at two different constant voltages (simulation).



Figure 3: Zoom of the initial current peak in Fig. 2 (left-hand side).



**Figure 4:** Snapshots of the current filament profile along a horizontal cut-line (cf. Fig. 3).

SIMULATION OF SEMICONDUCTOR PROCESSES AND DEVICES Vol. 12 Edited by T. Grasser and S. Selberherr - September 2007

explained as follows: After the spot, from where the filament had its origin, has cooled down, avalanche multiplication sets on again. The higher the voltage applied, the less this spot has to cool down in order to be ready for restarting filament generation, i.e. the shorter is the period between subsequent current peaks.

The current filament moves towards the region with a higher avalanche capability (left-hand side of the VLD structure). This is caused by avalanche-generated electrons and holes, which modulate the electric field not only in the region of maximum current density. Fig. 7 shows the electric field profile along a vertical cut at 125 µm for two different times: At  $t = 2.03 \mu s$  the maximum of the current filament is located at 130 µm (cf. Fig. 4), but the electric field exceeds the critical value already at 125 µm due to its dynamically steepened peak. For a further analysis of the interplay between reduced avalanche robustness due to a dynamic field modulation and higher robustness contributed by the inner cells, we performed simulations with a slightly larger thickness of the device structure resulting in an increase of the breakdown voltage underneath the front contact area. We observe a similar sequence of current peaks as shown in Fig. 2, but now the current filament moves only slightly to the left (Fig. 8). While this region heats up, the applied constant voltage is no longer high enough to maintain impact ionization. The remaining current concentrates at the original location of avalanche breakdown again and disappears with time due to selfheating.



**Figure 5:** Temperature distribution for  $t = 2.04 \ \mu s$  (cf. Fig. 3 and Fig. 4).



**Figure 7:** Electric field profile along a vertical cut-line at 125 μm for two different times (cf. Fig. 4).



**Figure 6:** Temperature distribution for  $t = 2.10 \ \mu s$  (cf. Fig. 3 and Fig. 4).



**Figure 8:** Current filament profiles (normalized to their maximum value) along a horizontal cut-line for different times t1 – t4 for a VLD structure with a slightly increased thickness.

## 3 Measurement

Fig. 9 shows the time-dependent current waveforms measured on IGBT test structures with VLD edge termination under avalanche breakdown conditions, with the applied voltage kept constant. We observe time-periodic distinct peaks, the number of which per time interval is increasing with rising voltage (not shown here). The measured current peaks are much broader compared to those simulated. Presumably, avalanche breakdown in the real device does not only occur at the four corners of the cell array resulting in broader current peaks (cf. Fig 10). But apart from this detail, the measured current waveforms conform with the simulations. Therefore we conclude that the VLD edge termination around the IGBT cell array is the location of initial current filamentation. The self-extinguishing of the filament prevents the IGBT cell array from being destroyed.

# 4 Conclusions

We analyzed the role of "variation of lateral doping" (VLD) edge termination structures with respect to the ruggedness of IGBT cell arrays. In the avalanche breakdown regime, we observe time-periodically traveling and self-extinguishing current filaments. This mechanism prevents the device from running into destruction and, thus, increases their ruggedness. The simulations are satisfactorily confirmed by experiments.



measured on an IGBT cell array with VLD edge termination (test structure) for constant applied voltage.



800

sample b

Figure 10: Zoom of one of the current peaks (measurement).

#### References

- A. Icaza-Deckelmann, G. Wachutka, F. Hirler, J. Krumrey, R. Henninger, "Failure of multiple-cell power DMOS transistors in avalanche operation", Proceedings of the 33rd European Solid-State Research Conference (ESSDERC) 2003, Estoril, Portugal, pp. 323-326.
- [2] DESSIS TCAD, distributed by Synopsis.

192