Transient Characterization of Interface Traps in 4H-SiC MOSFETs

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Abstract

High density of interface traps at the SiC-SiO_2 interface gives rise to lower mobilities and currents in SiC MOSFETs. Detailed investigations are performed to measure and characterize these interface traps using experimental and modeling methods [1-3]. Recent measurements of threshold voltage instabilities by fast I-V methods have shown that the SiC-SiO_2 interface not only contains fast interface traps, but also slower near-interface and oxide traps [4, 5]. Steady state modeling and simulations cannot characterize the effects of each of these defects. We have hence developed a detailed time dependent modeling scheme for dynamic interface trap occupation, and incorporated it into our 2D transient device simulator. We use the transient modeling to separate out and individually characterize interface, near-interface and oxide traps in 4H-SiC MOS devices.

1 Introduction

SiC MOSFETs have large trap densities at the SiC-SiO_2 interface. We have developed an algorithm that can be used to study the dynamics of these traps. The algorithm uses a time dependent trapping and generation-recombination model which provides information of trap occupation as a function of time and energy. While the model provides details of the dynamics of trapping in energy and time, it also fits into standard device simulation methodologies. Here, this model is presented, and the energy and time dynamics of trap occupation are described and experimentally validated.

2 Time Dependent Trap Occupation

The filling/emptying of a trap at the SiC-SiO_2 interface can be expressed as a generation-recombination phenomenon between a trap and a surface electron in the device. We generalize the Shockley-Reed-Hall generation-recombination equations [6] to time dependent trapping in a SiC MOS system. The rate at which surface electrons with energy E are captured by traps located at energy E_t is given as:

$$dU_c(E,E_t) = \left[(1-f_t(E_t))D_{it}(E_t)dE_t\right]\left[f(E)N(E)dE\right]c_n(E,E_t) \qquad (1)$$

Where, $f_t(E_t)$ is the occupation probability of a trap at E_t, $D_{it}(E_t)$ is the trap density of states, $f(E)$ is the occupation probability of an electron state at energy E, $N(E)$ is the

conduction band electron density of states, and $c_n(E, E_t)$ is the energy dependent capture probability which incorporates the trap cross-section.
Similarly, the emission rate can be written using $e_n(E, E_t)$ as the energy dependent emission probability as:

$$dU_e(E,E_t) = [f_t(E_t)D_{it}(E_t)dE_t][(1-f(E))N(E)dE]e_n(E,E_t) \quad (2)$$

Writing the capture probability as a product of the energy dependent trap cross-section and average thermal velocity ($\langle A_{it}(E_t)\cdot v_{th}\rangle$), and equating the capture and emit rate in steady state, after algebraic manipulation, the net recombination rate ($dU_{ce} = dU_c - dU_e$) at trap energy E_t becomes:

$$\boldsymbol{dU_{ce}(E_t) = [D_{it}(E_t)A_{it}(E_t)\Delta E_t]\langle v_{th}\rangle\left[(1-f_t(E_t))\cdot n - \frac{1}{2}f_t(E_t)N_c \exp\left(\frac{E_t - E_C}{k_B T}\right)\right]} \quad (3)$$

Here, E_C is energy at the conduction band edge, n is the surface electron concentration, and N_c is the effective conduction band density of states.

The density of occupied traps at energy E_t and time step k+1 depends on the occupied traps at the previous time step ,k and the net recombination occurring at energy E_t in the time interval Δt. This occupied trap density is written as:

$$dN_{it}(E_t)^{k+1} = dN_{it}(E_t)^k + \Delta t \cdot dU_{ce}(E_t)^{k+1} \quad (4)$$

3 Interface, near-interface and oxide traps

This recombination model is suitable for the characterization of interface traps, near-interface and oxide traps. The near-interface and oxide traps get filled very slowly as compared to the interface traps in a SiC MOS system. Therefore, we incorporate the effects of near-interface and oxide traps by modeling them as traps spread towards the middle of the SiC bandgap and with small cross-sectional areas. Interface traps are modeled as having larger cross-sectional areas. So, their occupation occurs more quickly as compared to the near-interface and oxide traps.

4 Simulation Method and Results

We developed a SiC MOS device simulator that incorporates this model. First, steady state simulations and comparison to experiment are performed to extract the interface trap density of states (Figure 1(a)) [3]. We note that the extracted density of states curve also includes near-interface and oxide traps. Then transient simulations with gate-voltage pulses with various voltage levels, rise/fall times, and frequencies are carried out to characterize the interface, near-interface and oxide traps.

Figure 1(b) shows the simulated and experimentally measured transient current flowing through a 4H-SiC MOSFET on application of a 0-5V gate pulse with a rise time of 100ns. Initially, the current rises very quickly and reaches a peak because the interface traps respond slowly as compared to the inversion layer formation. As the traps get occupied, the current decays to its steady state value as conduction electrons become trapped. The rate of this current decay and trap occupation is proportional to

the energy dependent cross-sectional area of the interface traps, which has been extracted by fitting the simulated transient current response to experiment.

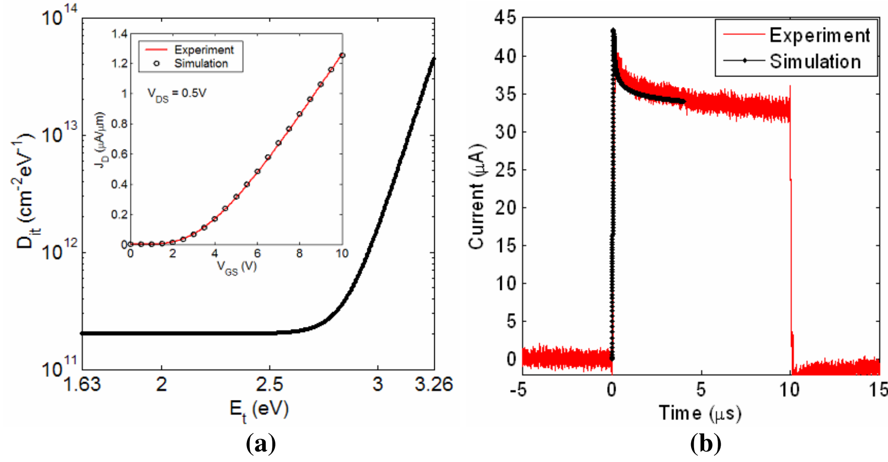

Figure 1. **(a)** Extracted $D_{it}(E_t)$ profile for acceptor type traps in a 4H-SiC MOSFET from steady state I_D-V_G comparison to experiment. **(b)** Experimental and simulated transient current responses of a 4H-SiC MOSFET. The simulated curve (shown for 4μs) follows the experimental measurement, thereby verifying the generation-recombination model and allowing us to extract the energy dependent trap cross-sectional area profile.

The dynamics of the trap occupation in a 4H-SiC MOSFET not only depends upon the trap density of states, but also upon the trap cross-section. From our simulations and comparison to experiment, we extracted the trap cross-section area profile as shown in Figure 2(a). The traps lying below 2.6eV are always completely filled and hence do not play a role in the transient response of the system. So, we do not include their cross-section area in the figure. The traps lying near the band-edge behave as fast interface traps, whereas those lying towards the middle of the bandgap behave as slower deep traps, near interface traps, and oxide traps.

Figure 2(b) shows the occupation probability of the interface traps for different time instances. At the beginning of the pulse, the trap probability follows a Fermi-Dirac distribution with the low energy traps completely occupied and traps near the band edge unoccupied. As the gate pulse rises, there is a sudden rise in the surface electron concentration. The traps near the band-edge get occupied first because they have larger cross-sectional areas, and also because they were empty to begin with. Therefore, they limit the peak value of the transient current. As time goes on, the traps further away from the band-edge start getting occupied, whereas those near the band-edge settle down to their final occupation levels. This causes the slow decay in the current seen in Figure 1(b). Finally a new Fermi-Dirac type distribution state with a higher occupation level corresponding to the new gate voltage emerges. After this there is no change in the trap occupation and the current becomes constant. Thus, the system reaches steady state.

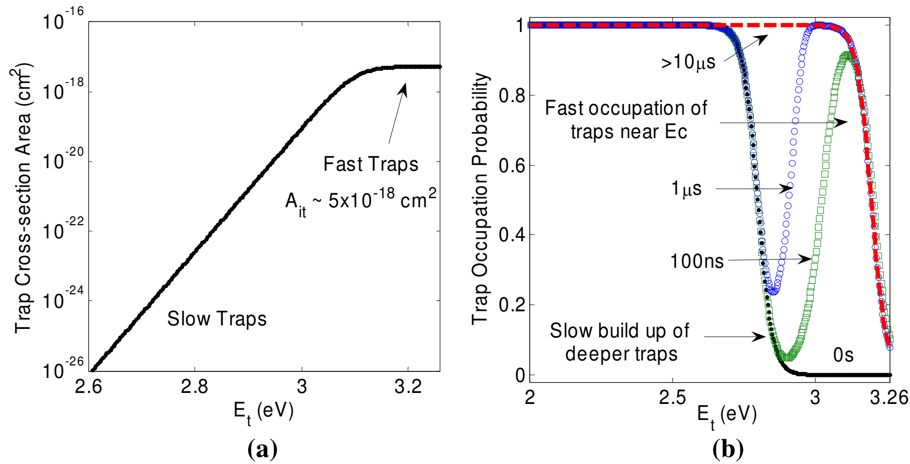

Figure 2. (a) Energy dependent trap cross-section area profile that gave simulated transient current comparable to the measured characteristics. **(b)** Occupation probability of the interface traps shown at different time instances. At t=0s, a Fermi-Dirac distribution with a Fermi level of about 2.8eV is seen. At t=100ns, the fast traps near the conduction band edge get occupied. At t=1μs, more of the deep traps are occupied. At some time t>10μs steady state is reached with the Fermi level at about 3.2eV.

5 Conclusion

A method for characterization of interface, near-interface and oxide traps in SiC MOS systems using transient modelling and simulation in conjunction with experiment is proposed. The model explains current transients and shift in threshold voltage observed during fast I-V measurements in 4H-SiC MOSFETs. Characterization of energy dependent density of states and capture cross-sections of interface traps has been achieved. This device modelling method can be applied SiC MOS and high-k devices to evaluate their dynamic performance.

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