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Analysis of Silicon Dioxide Interface Transition Region in MOS Structures

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Abstract

We study the Si(100) inversion layer quantisation, capacitance and tunnelling characteristics in the case of a gradual band gap transition at the Si/SiO_2 interface. A linear band gap transition of 0.5 nm at the SiO_2 side results in nearly 20% redistribution of carriers from the 2-fold to the 4-fold degenerate valley, due to the greater wave-function penetration and sub-band level lowering for the 4-fold valley. The gate capacitance is enhanced by up to 12% for a 1.0 nm nominal oxide thickness, and the direct tunnelling current density increases by an order of magnitude.

1 Introduction

The exact physical arrangement of atoms and the chemical composition at the common boundary between SiO_2 and Si remains disputable, but the energy levels of the electronic states that directly affect the electronic properties of the interface, are determined to a good agreement [1, 2, 3, 4, 5]. Additional electronic states, energetically aligned closer to the Si conduction band, are found in the first $2-6$ Å from the end of the ordered Si structure. This implies a gradual formation of a sufficiently large band gap in the SiO_2 [2, 3], and stipulates a gradual transition of the dielectric permittivity [4].
The effect of a gradual interface band-gap transition on the electron mobility and energy quantisation in metal-oxide-semiconductor (MOS) structures has been briefly addressed by Stern [6], who predicted lowering of the sub-band energies, and suggested part of the scattering usually attributed to surface roughness is due to the charge in the transitional oxide. Recently Watanabe accounted for the interface transition region (TR) when estimating the tunnelling oxide effective mass and effective oxide thickness [7]. However, a more detailed study of the MOS inversion layer with consideration of the TR is still missing. Here we obtain a semi-quantitative estimate for the effect of gradual interface band-gap transition on the inversion layer quantisation, capacitance and tunnelling characteristics.

2 Simulation Approach

This study is based on a 1-D self-consistent solution of the Poisson and Schrödinger equations (SE), using a modified version of Schred 2.0 solver [8]. The implementation delivers wave-function solutions subject to open boundary conditions (OBC) with a non-zero density in the oxide [9]. A 6-ellipsoidal band structure is adopted for the Si conduction band, and a single, parabolic band structure with effective mass $m_{ox} = 0.5m_0$ approximates the SiO_2. Further modifications allow us to model a gradual change in the material parameters in the transition region. Here we assume linear variation of the band gap. The dielectric permittivity and effective mass in the TR are those of SiO_2. Quasi-bound-states (QBS) lifetime approach is used to calculate direct tunnelling of electrons, consistent with the transfer-matrix technique for solving the SE [10].

3 Results and Discussion

We study a set of 1-D MOS structures with SiO_2 dielectric of thickness in the range of $1.0 - 1.8$ nm. The p-Si (100) substrate is uniformly doped to 2×10^{18} cm^{-3} and a metal gate with a 4.1 V work function is assumed, to avoid poly-Si depletion. We analyse the effect of a band-gap transition region (TR) of width in the range of $0.2 - 0.5$ nm, and compare solutions of the SE, subject to three different boundary conditions for the envelope wave function at the Si/SiO_2 interface - closed boundary condition with abrupt interface (CBC), open boundary with abrupt interface (OBC, abr.), and open boundary with gradual transition of the band gap (OBC, gr.). Fig. 1 shows the conduction band profile and electron density distribution at 0.9 V gate bias. The increase in the total

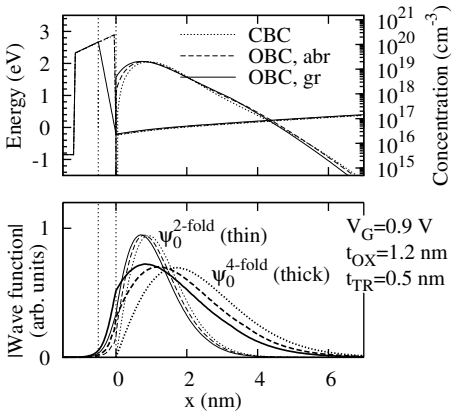

Figure 1: Conduction band profile and electron density for different boundary conditions for the wave-function (above), and normalised wave-functions (modulus) for the lowest sub-band in the 2- and 4-fold degenerate valleys (below).

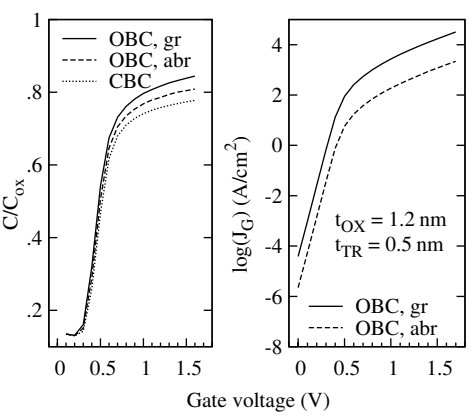

Figure 2: $C - V$ (left) and $J_G - V$ (right) characteristics of the structure, for different boundary conditions (BC) for the envelope wave function - closed (CBC), open with abrupt interface (OBC, abr.), and open with gradual interface (OB, gr.).

charge density in the inversion layer is due to the OBC for the wave-function solution. The gradual change in the band gap further relaxes the confinement at the left side of the quantum well. Although the average distance of the peak inversion charge has relatively minor change, there is a significant shift towards the interface of the peak density of electrons occupying the lowest 4-fold sub-band. The increased charge density at the nominal interface, $x = 0$, enhances the gate capacitance in the simulation with graded interface, as shown on Fig. 2 (left). Fig. 2 (right) also shows an increase of the gate current by an order of magnitude due to the non-abrupt shape of the tunnelling barrier.

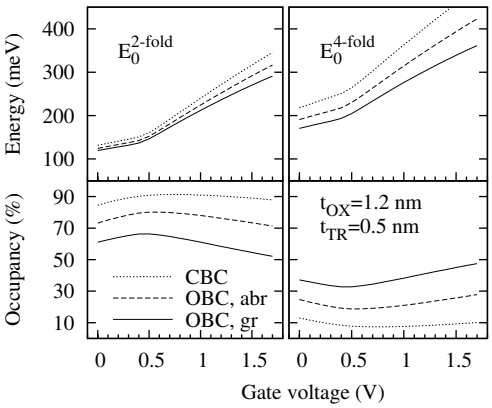

Figure 3: Sub-band energy and sub-band occupancy (percentage of the total inversion charge density) dependence on gate voltage, for different boundary conditions for the wave-function.

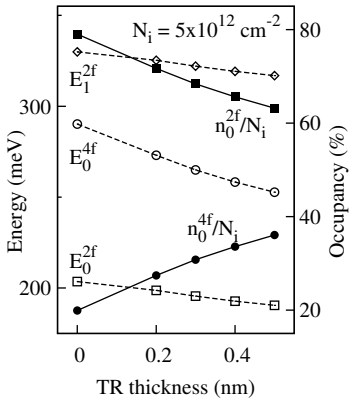

Figure 4: Sub-band energy and occupancy dependence on transition region (TR) thickness, for a constant inversion charge, N_i.

Figure 3 shows the change in sub-band energy levels and sub-band occupancy for the lowest sub-bands in the 2-fold and 4-fold degenerate valleys, as a function of gate voltage. The effect of band-gap transition on the 4-fold degenerate valley is stronger due to the greater widening of the well for higher energies, and the lower quantisation effective mass. The dependence of sub-band energy and occupancy on the TR thicknesses is shown on Fig. 4, where the same amount of inversion charge is maintained for all TR widths. For the widest simulated TR the occupancy of the lowest 4-fold sub-band (E_0^{4f}) increases by nearly 20% at the expense of the depleted 2-fold ground state (E_0^{2f}). We find that these results are practically independent of the simulated nominal t_{OX}. This could be explained with the rapid attenuation of the wave-function once the SiO_2 band-gap fully develops, and implies that the exact profile of the conduction band in the TR is deterministic for the magnitude of the simulated effects.

Figure 5 shows the relative effect of TR thickness on the direct tunnelling current at a nominal oxide thickness of 1.0 nm. Tunnelling from the 4-fold sub-bands is enhanced stronger due to the relative occupancy increase and barrier thinning, compared to the 2-fold sub-bands, and to the case of an abrupt interface, respectively. We find that increasing t_{OX} to 1.8 nm does not change the ratio plotted on Fig. 5.

The gate capacitance dependence on the TR width is shown on Fig. 6, for a 1.0 nm

nominal oxide thickness. The peak of the relative difference, with respect to an abrupt interface, is nearly 12% for the widest TR. We find that the voltage to which this peak is correlated increases for thicker oxide, however the magnitude of the peak decreases.

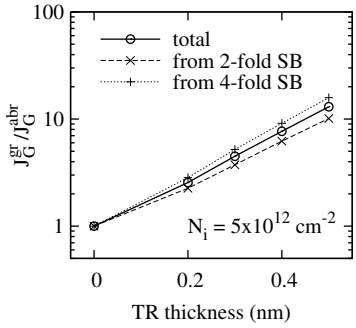

Figure 5: Direct tunnelling current density dependence on transition region (TR) thickness, for constant inversion charge, N_i.

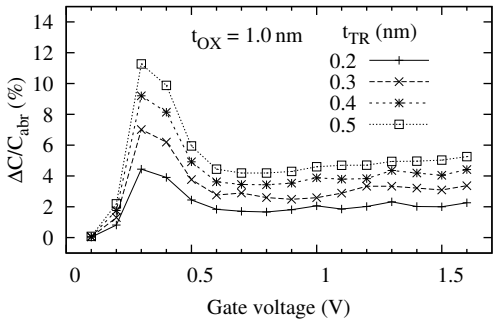

Figure 6: Gate capacitance relative difference, with respect to abrupt interface, for various transition region thicknesses, t_{TR}, and given oxide thickness, t_{OX}.

4 Conclusions

We elaborated on the effects of gradual Si/SiO_2 interface band-gap transition on the MOS inversion layer. The confinement relaxation due the gradual barrier lowers the quantisation levels and causes redistribution of electrons from the 2-fold, to the 4-fold degenerate valley (20% for the widest TR). The widening of the TR significantly enhances the gate capacitance and, exponentially, the direct tunnelling current. The sensitivity of the results on the TR thickness, rather than the oxide thickness, implies the exact conduction band profile largely determines the magnitude of the observed effects.

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