SIMULATION OF SEMICONDUCTOR PROCESSES AND DEVICES Vol. 12 129
Edited by T. Grasser and S. Selberherr - September 2007

Device Design and Scalability of an Impact Ionization MOS Transistor with an Elevated Impact Ionization Region

Eng-Huat Toh, Grace Huiqi Wang, Lap Chan, Ganesh Samudra, and Yee-Chia Yeo.

Silicon Nano Device Lab., Dept. of Electrical and Computer Engineering,
National University of Singapore (NUS), Singapore 117576.
Phone: +65 6516-2298, Fax: +65 6779-1103, Email: yeo@ieee.org

Abstract

This paper reports a novel L-shaped Impact-ionization MOS (LI-MOS) transistor structure that achieves a subthreshold swing of well below 60 mV/decade at room temperature and operates at a low supply voltage. The device features an L-shaped or elevated Impact-ionization region (I-region) which displaces the hot carrier activity away from the gate dielectric region to improve hot carrier reliability and V_T stability problems. Device physics and design principles for the LI-MOS transistor are detailed through extensive two-dimensional device simulations. The LI-MOS transistor exhibits excellent scalability, making it suitable for augmenting the performance of standard CMOS transistors in future technology generations.

1 Introduction

CMOS device scaling faces formidable challenges. Continuous reduction of V_T with device scaling results in higher subthreshold leakage current I_{off} and static power consumption, and is limited by the non-scalability of the subthreshold swing S. To realize S of less than 60 mV/decade at room temperature, a device structure [1] that modulates the breakdown voltage of a gated p-i-n structure to switch between the off and on states was proposed. The Impact-ionization MOS (I-MOS) device exploits the avalanche effect of impact ionization to realize a steep increase of current from the off-state to the on-state. An alternative device structure, the L-shaped I-MOS (LI-MOS) [2] that uses elevated or L-shaped Impact-ionization region (I-region) relocates the impact ionization activity away from the gate dielectric region, thus reducing V_T instability due to hot carriers. A selective epitaxial growth (SEG) which forms the elevated I-region allows accurate dopant profile engineering and easy controllability and scalability of the I-region dimensions. In addition, the LI-MOS device has a compact self-aligned device structure to improve packing density and is also CMOS-process-compatible. This paper reports insights into the device physics and key device design principles of the LI-MOS transistor, and explores its scalability for future technology generations.

2 Device Structure and Physics

The LI-MOS transistor has a L-shaped I-region comprising an elevated I-region with thickness T_I and resistance R_V, and a horizontal I-region with length L_S and resistance

R_H (Fig. 1(a)). The L-shaped I-region has a total length $L_I = T_I + L_S$. The horizontal portion of the I-region has a p-type doping concentration N_B, and the elevated I-region has a doping concentration of 1×10^{13} cm^{-3}. The doping concentrations in the n^+ drain and p^+ source are 2×10^{20} cm^{-3}. Synopsys TCAD tools were used to study the device physics and design principles. Self-consistent impact ionization model [3] and band-to-band tunneling model were used with other essential models to accurately simulate sub-100 nm gate length devices at 300 K.

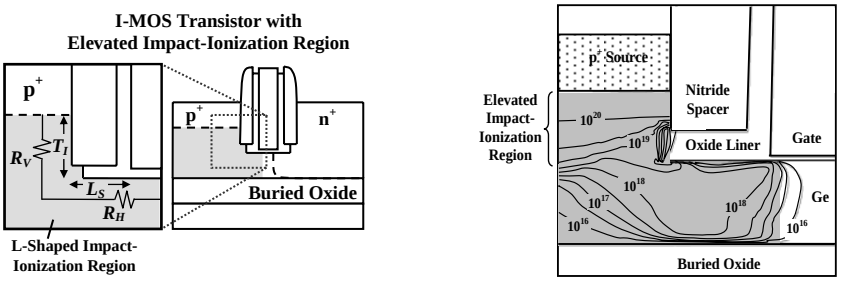

Fig. 1 (a) Schematic of an n-channel I-MOS Transistor with an Elevated Impact-ionization region (I-region), showing the equivalent resistances and dimensions in the I-region. **(b)** The concentration contour plot of holes generated by impact ionization for a Ge LI-MOS is shown. The majority of the holes generated are confined to the I-region (Gray).

The I-MOS transistor operates in the two states. In the off-state, the source is at a negative bias with the drain at a positive bias. Hence, the off-state current is the drift of the minority electron carriers. In the on-state, the gate induces sufficient band bending in the I-region to cause impact-ionization. Fig. 1(b) depicts the concentration contours of holes generated by impact-ionization in a Ge LI-MOS. By altering the resistance values of R_V and R_H (i.e. N_B, T_I, and L_S), hot carrier reliability could be improved by displacing the impact ionization activity away from the gate dielectric region. For instance, increasing N_B causes more voltage drop across R_V and increases the electric field in the elevated I-region. As a result, hot carrier activity is reduced in the horizontal I-region, and most of the hot carriers are confined in the elevated I-region. In this study, the LI-MOS device is formed on a Germanium-on-Insulator (GOI) substrate to exploit the high impact ionization coefficient of Ge. The benefits of Ge comes not only from lower breakdown voltage, but also much lower off-state current I_{off} and higher on-state current I_{on}.

3 Device Design and Optimization

Fig. 2(a) shows the dependence of I_D-V_G on N_B and excellent subthreshold swings of ~1 mV/decade for Ge n-channel LI-MOS transistors. V_T decreases with increasing N_B, as illustrated in Fig. 2(b) unlike in conventional MOS transistors. Increasing N_B leads to a greater voltage drop across the elevated I-region, therefore leading to higher electric field, increased impact ionization, and reduced V_T. The depletion width and R_H depend inversely on N_B which causes V_T to decrease. In addition, I_{off} is found to be lower in devices with lower V_T (higher N_B) than in devices with higher V_T (lower N_B). See Fig. 3(a). This is explained by a well-known inverse proportionality of I_{off} to N_B

for a p-i-n diode [4]. Unlike the lateral I-MOS [1] where changing the substrate doping N_B affects the whole I-region directly, the intrinsic region could be maintained in the elevated I-region while optimizing N_B for better breakdown characteristics in the LI-MOS. Fig. 3(b) shows that V_T increases with increasing T_I, for various L_S values. An effective way to control V_T is through control of the thickness of the elevated I-region T_I by SEG. The use of SEG automatically miniaturizes the LI-MOS as there is no area penalty for including the elevated I-region. L_S may also be employed to tune V_T over a wide range if needed. However, I_{off} increases rapidly as L_I becomes comparable to L_G (Fig. 4(a)). Nevertheless, higher N_B allows simultaneous realization of lower V_T and lower I_{off}, enabling device operation at lower V_{DD} and yet out-perform the I_{off}-I_{on} specifications in the International Technology Roadmap for Semiconductors (ITRS-2006) [5].

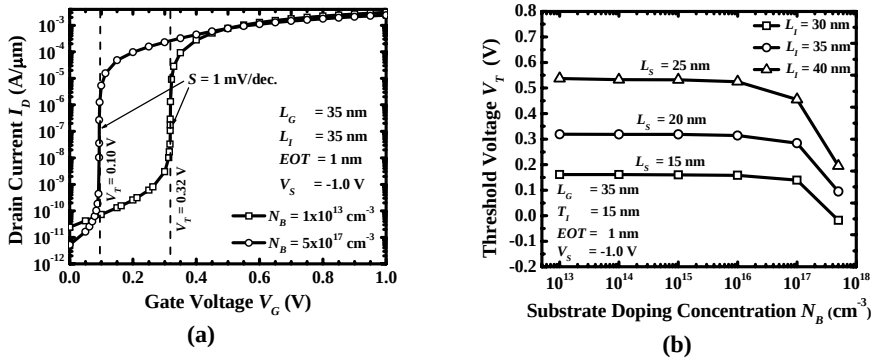

Fig. 2 (a) Simulated I_D-V_G plot of Ge n-channel LI-MOS transistors with two different substrate doping concentrations N_B, showing a 1 mV/decade transition between the off- and on- states. **(b)** Plot of threshold voltage V_T versus substrate doping concentration N_B for various length L_S, keeping T_I fixed at 15 nm. The L-shaped I-region has a total length $L_I = T_I + L_S$. A longer L_S causes V_T to drop faster as N_B increases.

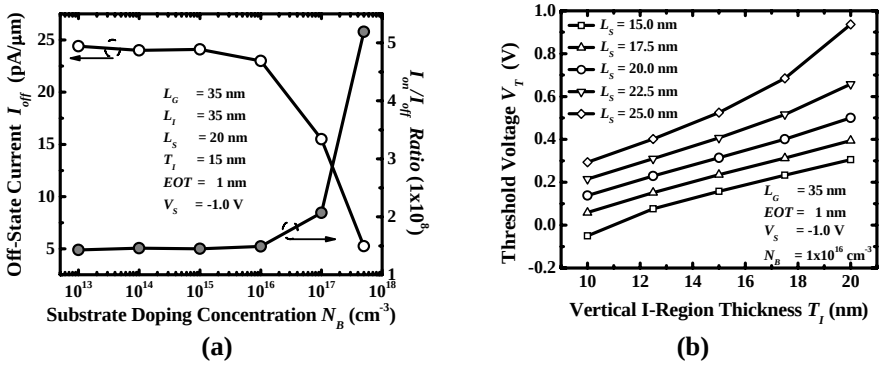

Fig. 3 (a) Plot of I_{off} and I_{on}/I_{off} ratio as a function of substrate doping concentrations N_B. I_{off} decreases as N_B increases. **(b)** Threshold voltage V_T generally increases with increasing T_I. L_S and T_I are two adjustable parameters that allows for the flexibility of V_T tuning.

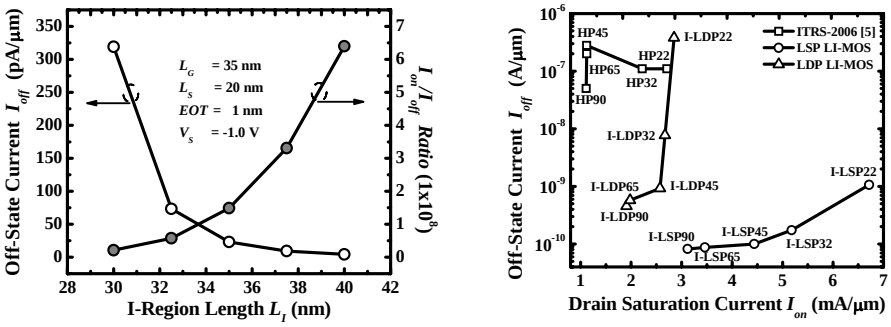

Fig. 4 (a) Plot of I_{off} and I_{on}/I_{off} ratio as a function of I-region length L_I. This also causes the I_{on}/I_{off} ratio to decrease. **(b)** Superior capabilities of the Ge I-MOS technology using elevated I-region, as compared with projected I_{off} and I_{on} targets of High-Performance (HP) CMOS technology nodes [5].

4 Device Scalability

To illustrate the scalability of the Ge LI-MOS transistor, simulations were carried out for each I-MOS technology node. An I-MOS technology node employs device structure parameters, e.g. gate length L_G, that are identical to those in the corresponding high-performance (HP) logic technology node [5], but T_I and L_S are used to optimize device performance. I-MOS transistors may be designed to achieve Low Static Power (LSP) or Low Dynamic Power (LDP) while maintaining high performance. I-MOS for LSP applications, i.e. I-LSP technology, may employ the same V_{DD} as those in the corresponding HP CMOS technology node. Fig. 4(b) shows that I-LSP transistors demonstrate superb performance (lower I_{off} and higher I_{on}) that exceeds the ITRS-2006 projections. I-MOS for LDP applications, i.e. I-LDP technology, may employ aggressively reduced V_{DD} while satisfying the I_{on} specifications in ITRS-2006 [5].

5 Conclusion

The Ge LI-MOS, or I-MOS with an elevated impact-ionization region, is a CMOS-process-compatible technology that is promising for augmenting the performance of conventional CMOS transistors. Its L-shaped impact-ionization structure allows the diversion of hot carrier activity away from the gate dielectric region, a critical improvement over existing I-MOS structures. The Ge LI-MOS device has excellent scalability in future technology nodes, enabling very significant reduction of power consumption in high-performance logic applications.

References

[1] K. Gopalakrishnan *et al.*, *IEDM Tech. Dig.*, pp. 289-292, 2002.
[2] E.-H. Toh *et al.*, *IEDM Tech. Dig.*, pp. 971-974, 2005.
[3] S. Selberherr, *Springer-Verlag*, 1984, ISBN 03878006.
[4] B. J. Baliga, *J. Wiley*, pp. 407-419, 1987, ISBN 0471819867.
[5] ITRS 2006, http://www.itrs.net/