Impact of Two-Step Recessed SiGe S/D Engineering for Advanced pMOSFETs of 32 nm Technology Node and Beyond

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Abstract

The two-step recessed SiGe Source/ Drain (S/D) structure, which is one of the embedded SiGe S/D engineering techniques, is a leading candidate for advanced pMOSFETs from the viewpoint of good roll-off characteristics and high channel strain. In this paper, we reveal the merits of this technology for the application to the 32 nm technology node, including the methodology for suppressing the layout effect by TCAD analysis.

1 Introduction

The embedded SiGe Source/Drain (S/D) engineering [1 - 4] has been the key to realization of advanced pMOSFETs because of its ability to create strong channel strain that brings about significant mobility enhancement. However, it is accompanied by the degradation of short channel effect when SiGe S/D regions are close to the gate edge for higher channel stress. This is because p-type S/D region inevitably becomes deeper as shown in Fig. 1(a). To resolve this trade-off, the two-step recessed SiGe S/D structure [3] shown in Fig.1 (b) has been proposed. It can form both shallow p-type SiGe extensions and deep S/D regions simultaneously by epitaxial growth of SiGe. Thus, good roll-off characteristics are achieved while keeping high channel strain. Therefore, it has become an attractive scheme for future technology generations. In this paper, we report on TCAD analysis of two-step recessed SiGe S/D technology for optimizing its structure for the application to the 32 nm technology node. We have clarified its merit of high channel strain compared with the conventional embedded SiGe structure. In addition, the methodology for suppressing layout effect is presented.

2 Simulation Methodology

Synopsys TCAD tools [5] with internal calibrations are used. In stress simulation, silicon and SiGe regions are treated as isotropic elasticity with 169 GPa and 130 GPa Young's modulus, respectively. In device simulation, the drift-diffusion model with density-gradient quantum correction and Intel stress dependent hole-mobility models is used.
We first checked the simulation accuracy by comparing with existing experimental data of <110> channel pMOSFET with two-step recessed eSiGe (Ge=20 %) S/D. Here, boron in eSiGe extension and S/D regions is in-situ doped without ion implantation process. Simulated V_{th} roll-off and I_{on}-I_{off} characteristics are in good agreement with the experimental ones as shown in Fig. 2 which assures that the same simulation approach can be used for further investigation.

3 Simulation Results

Fig. 3 shows the parameters considered, namely, the depth of extension SiGe and its proximity to gate when optimizing two-step recessed SiGe structure. Here, the depth of deep SiGe is fixed at 60 nm. In Figs. 4(a) and 4(b), the stress values along channel direction, S_{xx}, below 2 nm gate oxide/ Si interface are shown as functions of the depth of extension SiGe. It is found that there is the optimum depth of extension SiGe for maximizing S_{xx} and the peak S_{xx} is obtained with deeper extension SiGe when the offset of deep SiGe is wider.

In Fig. 5, stress distribution of two-step recessed SiGe structure with extension depth of 30 nm and the conventional eSiGe one is shown. It is known that the smaller the cross-sectional area, the stronger the stress value is when the same force is applied to the material. Indeed, S_{xx} at the channel of two-step recessed structure is 1.8 GPa and higher than the 1.7 GPa of the conventional case as shown in Fig. 5(c). In the case of long gate length, the stress value of two-step recessed structure is weaker than that of the conventional structure due to the long distance from the extension SiGe/ Si interface to the center of gate (Fig. 6). Simulation results of channel stress on gate length are shown in Fig. 7. This figure indicates that the depth of extension SiGe should be shallow for obtaining the maximum channel stress as gate length shrinks. This would also be favorable from the viewpoint of controlling short channel effect.

For optimizing the two-step recessed SiGe structure, response surface model for the drive current, I_{on}, of metal gate pMOSFET at fixed off-leakage as functions of the depth of extension SiGe and channel concentration is generated as shown in Fig. 8. The simulated pMOSFET is with L_g=28 nm, and EOT=1.1 nm. Corresponding metal gate workfunction (WF) is also plotted. There is clear tendency for higher I_{on} to be obtained when the depth of extension SiGe is between 15 nm and 20 nm. At WF=5.1 eV which is 100 mV from the valence band edge and is expected to be achievable for 32 nm technology node, the optimum depth is 17 nm. This is shallower than the depth of 30 nm which gives maximum stress as shown in Fig. 4(b). It indicates that the optimization of S/D doping profiles for good cut-off characteristics is important in addition to increasing stress. Figs. 9(a) and 9(b) show the optimized doping profiles and I_d-V_g characteristics. Simulated I_{on} is 701 μA/μm at V_d=-0.9 V with I_{off} of 100 nA/μm. By the combination of metal gate and two-step recessed SiGe S/D with EOT of 1.1 nm, such high I_{on} can be expected. It clarifies that the two-step recessed SiGe S/D structure has great potential as a technology option for 32 nm node pMOSFETs.

With shrinking of the device width, W and S/D size, X, the strain at the channel decreases in embedded SiGe structure. Thus, it is important to consider the S/D size dependence. Here, the 3-D structures shown in Figs. 10(a) and 10(b) are analyzed. Fig. 10(c) shows that the stress values at X=70 nm and W=200 nm is one third of that for the non-STI-bounded structure. In order to obtain similar high strain, it is necessary to adopt another strain enhancement technology such as compressive stress gate capping liner. Fig. 11 shows the results of stress as functions of SiGe layer overgrowth height when combining two-step recessed SiGe with compressive stress liners. It shows that the lower the SiGe epi height and the higher the intrinsic stress value of liner, the higher the stress value in the channel is expected to be. Fig. 12 shows the simulated drive current at I_{off} of 100 nA/μm in the 3.5 GPa compressive liner case. It is possible to obtain high drive current even in fine-pitch structure by choosing the SiGe epi height close to 10 nm and combining it with high compressive gate capping stress liner.

4 Conclusion

We have demonstrated that two-step recessed SiGe S/D engineering is a promising candidate for the 32 nm technology by simulation. Its merit of high channel stress with shallow extension structure is analyzed and clarified. Moreover, we demonstrated how to improve the S/D size dependency by using 3-D stress and 2-D device simulations. Our simulation results will have a great impact on the design of planar pMOSFETs for 32 nm technology node and beyond.

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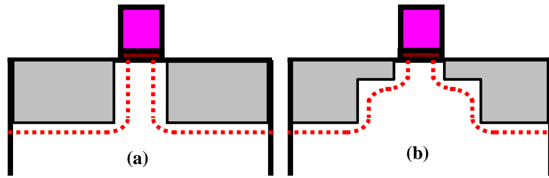


Fig. 1: Schematic illustration of conventional SiGe S/D (a) and two-step recessed SiGe S/D (b). Gray box regions and dotted lines indicate SiGe S/D and the p^+-n junction, respectively.

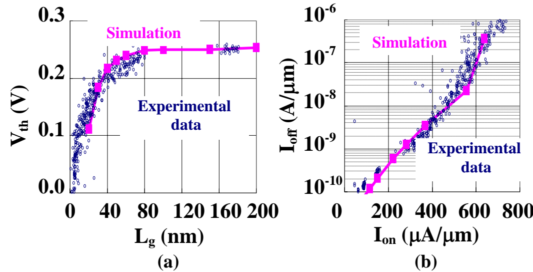


Fig. 2: Simulated and experimental V_{th} roll-off (a) and I_{on}-I_{off} (b) of two-step recessed SiGe S/D pMOSFET.

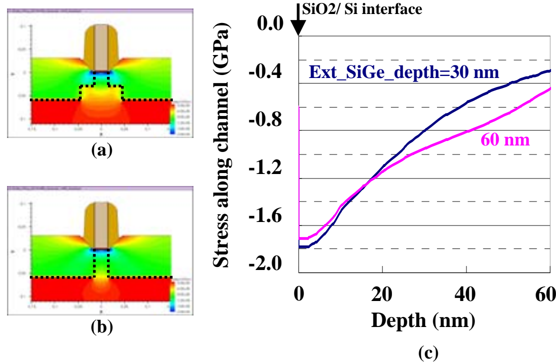


Fig. 5: Stress distribution in 28 nm gate pMOSFET with Ext_SiGe_depth of 30 nm (a) and 60 nm (b). Stress along the cut line at the center of gate is shown in (c).

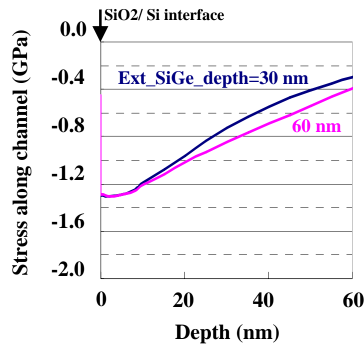


Fig. 6: Stress along the cut line at the center of gate in 50 nm gate pMOSFET.

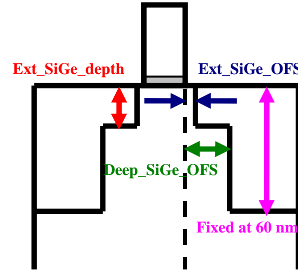
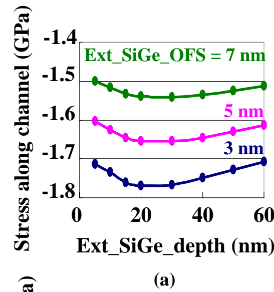


Fig. 3: Investigated parameters of two-step recessed SiGe S/D structure. The depth of deep SiGe S/D is fixed to 60 nm.



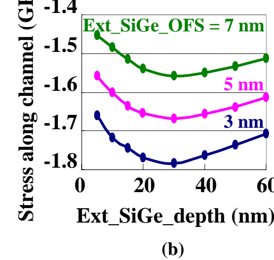


Fig. 4: Simulated stress applied to the inversion layer vs. the depth of extension SiGe in the case of Deep_SiGe_OFS of 15 nm (a) and 30 nm (b). Proximity of the extension SiGe to the gate edge is also varied.

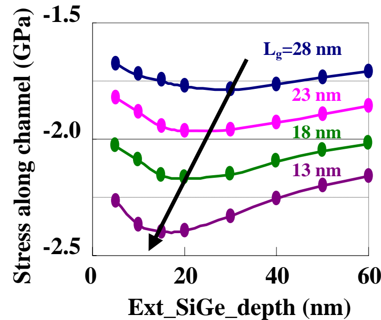


Fig. 7: Simulated stress applied to the inversion layer vs. the depth of extension SiGe when gate length (L_g) shrinks.

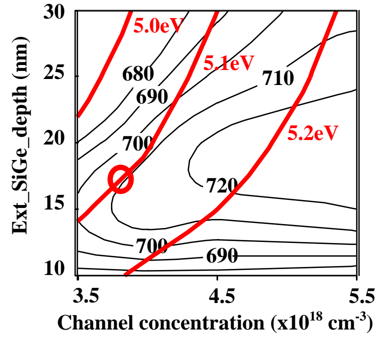


Fig. 8: Response surface contour of the drive current at I_{off} of 100 nA/μm and the metal gate workfunction (WF), which are designated by black and red lines, respectively. Red circle indicates the optimum point in the case of WF=5.1 eV.

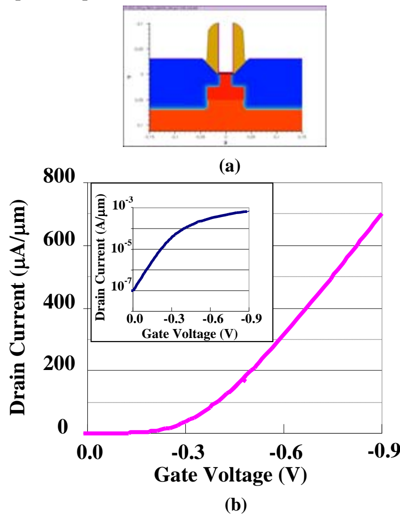


Fig. 9: Simulation results of dopant distribution and device structure (a), I_d-V_g characteristic (b).

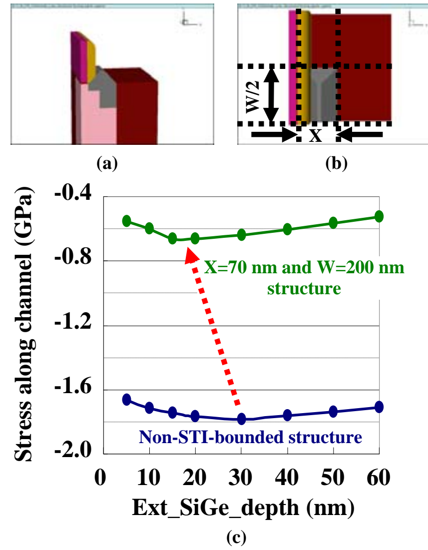


Fig. 10: Impact of layout effect on stress values in inversion layer. Simulated 3-D structure (a) and its top view (b), with X=70 nm and W=200 nm. Stress values in inversion layer vs. the depth of extension SiGe (c).

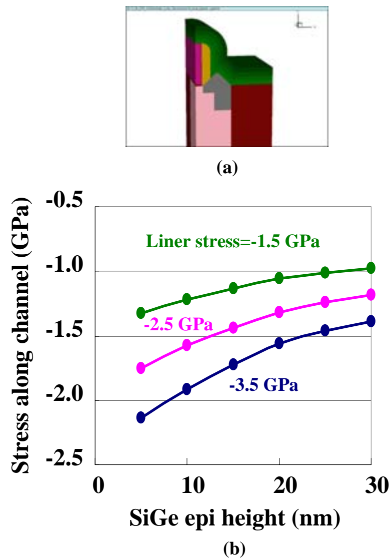


Fig. 11: 3-D structure (a) with combination of SiGe S/D regions and 40 nm thick compressive stress liner, and stress values in inversion layer simulated by shifting the SiGe epi height (b). Here, intrinsic stress values are variable.

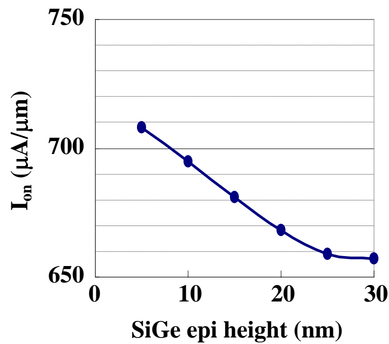


Fig. 12: The Simulated drive current of pMOSFET by using the combination of two-step recessed SiGe S/D and 3.5 GPa compressive stress liner, where V_{dd}=-0.9 V and I_{off}=100 nA/μm.