3D Stress, Process and Device Simulation: Extraction of the Relevant Stress Tensor

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Abstract

Three–dimensional (3D) stress, process and device simulation is performed for nMOSFETs with widths from 0.5 μm to 0.1 μm and gate lengths from 100 nm to 45 nm. Stress originates from a cap–liner with 2 GPa tensile stress. Drift–diffusion simulation with the linear piezoresistance model is employed considering either the position-dependence of stress or using a constant stress tensor obtained from averaging the stress in the source-side of the channel over a cuboid extending over the full device width. Considering a space–dependent or a constant stress tensor turns out to yield almost the same linear and saturation current enhancements. This permits to use the constant stress obtained from 3D stress simulation for much faster 2D process and device simulation. In particular, also only one band structure is needed for Monte Carlo device simulation.

1 Introduction

Stress engineering is currently the main approach to improve CMOS performance (e.g. [1]). Because of computational speed requirements, process and device simulation is to a large part still performed in 2D. As the device width shrinks, 3D simulation might first be routinely employed in mechanical stress investigations. When stress is significantly influenced by 3D effects, one question arising is on how to transfer the essential stress information to 2D device simulation. In Monte Carlo device simulation, it is also difficult to consider the whole spatial stress distribution, because every stress tensor involves a corresponding band structure. In this respect, it was recently found in 2D stress, process and device simulation that almost the same stress–induced current gain is obtained for gate lengths below 0.1 μm when either considering the whole stress distribution or a constant stress picked from the source–side of the channel [2]. It is therefore our aim to investigate by full 3D stress, process and device simulation, if a similar stress extraction is possible to reproduce the results from the complete space–dependence of stress. Last but not least, this provides important information about where stress most significantly influences electrical performance and hence where it should be optimized.

2 Simulation Example

We simulated bulk nMOSFETs with gate lengths in the range from 100 to 45 nm and device widths from 0.5 to 0.1 μm. Stress is introduced by a single 2 GPa tensile nitride

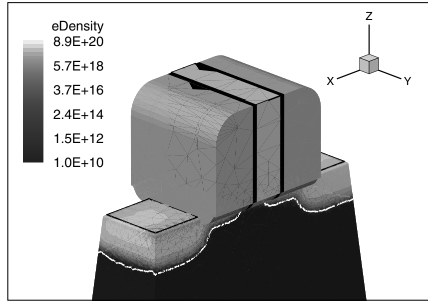

Figure 1: Electron density at V_{DS}=V_{GS} =1.1 V in the smallest simulated nMOSFET (gate length L_G=45 nm, width W= 0.1 μm). The crystallographic channel orientation is in $\langle 110 \rangle$ direction. STI and nitride cap layer are not shown.

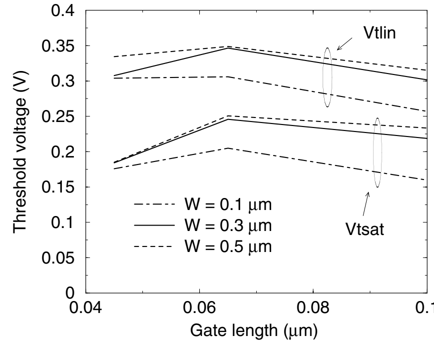

Figure 2: Linear and saturation threshold voltage roll–off curves for three different device widths.

cap layer. Otherwise, it is influenced by shallow trench isolation (STI).
A standard CMOS process flow was simulated with 2D channel implantation extruded in channel direction, while full 3D halo, lightly–doped drain (LDD) and source/drain implantation was performed. The corner rounding of the STI in width direction has a radius of 4 nm and a divot depth of 6 nm. Figs. 1 and 2 show the resulting structure and the corresponding threshold voltage roll–off curves, where the narrow channel width effect leads below a width of 0.3 μm to a threshold voltage lowering which is related to boron out–diffusion due to segregation.
Device simulation is done with the drift–diffusion approach using the linear piezoresistance model [3] applied both to bulk and surface mobility, but leaving the saturation velocity unchanged under stress. Quantum correction is accounted for by the modified local density approximation (MLDA).

3 Stress Simulation Results

Stress is introduced by deposition of a 100 nm thick nitride cap–layer film onto an (001)–nMOSFET with standard $\langle 110 \rangle$ channel orientation. The magnitude of the intrinsic tensile liner stress is 2 GPa and the poly height is 150 nm. Our mechanical simulations are based on release Z-2007.03 of the Sentaurus process simulator [4] and consider the anisotropic law of Hooke to relate the stress tensor to the strain tensor via the three independent elastic constants (C_{11}=167.5 GPa, C_{12}=65 GPa and C_{44}=80 GPa for silicon; for nitride a value of E=190 GPa is used for Young's modulus and a value of ν=0.3 for Poisson's ratio). The multi–layer model [5] for film deposition was not used. The influence of STI is considered by an equivalent intrinsic compressive stress of - 250 MPa and the length of diffusion (LOD) given as the distance between gate edge and STI is 220 nm.
Fig. 3 shows as one result of the mechanical simulation the spatial distribution of the xx–component of the stress tensor. The stress tensor obtained by averaging over a

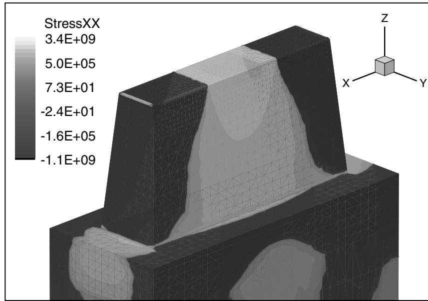

Figure 3: Spatial distribution of the xx–component of the stress tensor in the silicon body of the nMOSFET in Fig. 1 as resulting from a nitride cap–liner film with 2 GPa tensile stress.

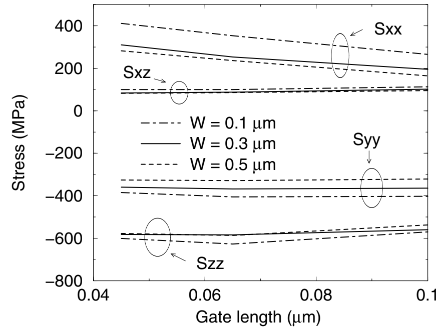

Figure 4: Gate length and width dependence of the stress tensor components. The components are averages over a cuboid around the source–side of the channel extending over the whole width.

cuboid centered around the pn–junction in the source–side of the channel and extending over the total width direction is displayed in Fig. 4. Note that the xy–component and the yz–component of the stress tensor averaged over this cuboid vanish due to symmetry. It is found that only the tensile stress in channel direction is sensitive to the gate length and increases appreciably upon scaling. Reducing the width increases the compressive stress in width direction, but increases also the tensile stress in channel direction.
Our main result on the linear drain current (Idlin) and the saturation drain current (Idsat) gains when using in drift–diffusion simulation either the constant stress tensor from Fig. 4 or the spatial stress distribution can be seen in Figs. 5 and 6. It turns out that (i) the current gains increase below a width of 0.3 μm due to the increase of the tensile stress in channel direction and that (ii) the constant stress tensor approximates well the results from the space–dependent stress tensors. There is only a certain underestimation of the current gains for the smallest width when using the constant stress which, however, is much smaller than the differences occurring when employing different transport equations or mobility models [2]. The small influence of the space–dependence of stress is due to a relatively weak stress variation in the channel for gate lengths below 0.1 μm compared to the case of long–channel devices and related to nanoscale–device currents being determined in the source–side of the channel.

4 Conclusions

We have performed 3D stress, process and device simulation and compared the stress–induced current enhancements when considering either the space-dependence of stress or using a constant stress picked from the source–side of the channel. It was found that using this constant stress is a good approximation. Hence, this result enables the combination of 3D stress with 2D device simulation as well as stress engineering based on Monte Carlo simulation.

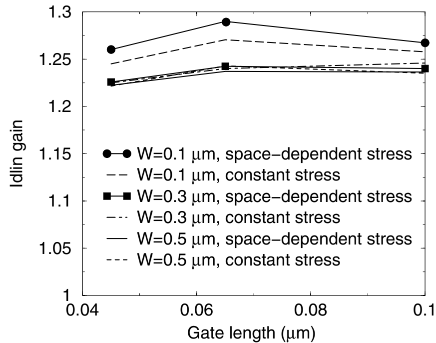

Figure 5: Stress–induced Idlin gain using the spatial stress distribution or the constant stress tensors of Fig. 4.

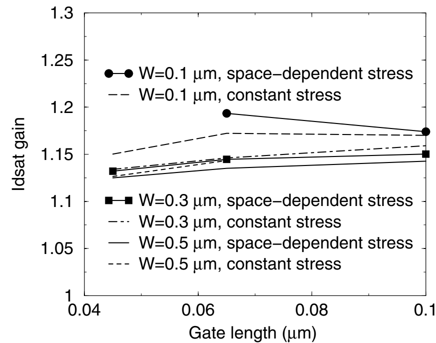

Figure 6: Stress–induced Idsat gain using the spatial stress distribution or the constant stress tensors of Fig. 4.

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