Analysis of Novel Stress Enhancement Effect Based on Damascene Gate Process with eSiGe S/D for pFETs

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Abstract

A novel stress enhancement effect based on the damascene gate process with embedded SiGe (eSiGe) S/D for pFET is analyzed in detail, using stress simulation and Ion measurement, for the first time. Removal of a dummy poly-Si gate eliminates the repulsive force from the gate with a resulting enhancement of lateral compressive stress from eSiGe S/D. The stress enhancement effect is proved by device fabrication and measurement. Furthermore, a new channel recess process is proposed and investigated. Channel recess further increases stress at the channel. This effect is also confirmed by measurement, resulting in 14% current enhancement.

1 Introduction

Strain-induced mobility enhancement technology, such as stress liner [1] or eSiGe S/D electrodes [2], is one of the key means for improving drive current (Ion). Inversion thickness (Tinv) scaling using metal/high-k gate stack is another important method of obtaining higher Ion with lower gate leakage level. We have already reported high performance and low-power CMOS technologies using the damascene metal/high-k gate process, or the gate last process, with strained channels [3]. In this paper, a detailed analysis of the Ion enhancement effect in pFET with damascene gate process and eSiGe S/D is performed. We found, for the first time, a superior stress enhancement effect based on this process. Using stress simulation and Ion measurement, the stress enhancement effect is compared with a conventional gate first process using eSiGe S/D. In addition to this fundamental investigation, we propose a new channel recess structure using damascene gate and eSiGe S/D, which achieves additional stress and current enhancement.

2 Stress enhancement for damascene gate process

Fig. 1 shows a schematic picture of the stress enhancement effect for the damascene gate process. In this process, a dummy poly-Si gate is initially formed on the Si substrate and then replaced by a metal gate. When the dummy poly-Si gate exists after eSiGe formation, the lateral compressive stress from eSiGe is reduced by the repulsive force from the gate. Removal of the dummy gate eliminates the repulsive force and thereby enhances the lateral stress at the channel. Figs. 2(a) and (b) show lateral stress distribution along A to B of Fig. 1(b) for L=40nm and L=60nm,

respectively. As can be clearly seen, compressive channel stress increases significantly after dummy gate removal for both cases.
In order to verify this stress enhancement effect, we fabricated devices and compared drive currents. The original damascene gate process (gate last process) forms metal/high-k gate stack after dummy gate removal. However, in order to avoid discrepancies between the poly-Si and metal gates, a poly-Si gate was formed again using the damascene process. The gate first process simply skips the dummy gate removal and the new poly-Si gate formation. The detailed process is reported in [4]. Fig. 3 shows 1/Tinv dependence of current at Ioff=100nA/um for linear and saturation region, where Tinv is the electrical oxide thickness at inversion state (Vg=-1.0V). From this measurement, there is almost no difference between gate first and gate last processes without eSiGe. With eSiGe S/D, the linear current (Id_lin) for the gate first process is enhanced by 84.2%. On the other hand, the enhancement for the gate last process is 115%. Since Id_lin enhancement corresponds approximately to the mobility enhancement [5], we estimated the mobility enhancement by bulk-Si piezo model [6] using average stress at the channel. By this estimation, we got 60% and 70% enhancement for the gate first and the gate last process, respectively. The difference between simulation and measurement may come from the limitation of the bulk piezo model since the model is acceptable only for small stress and does not include the inversion layer effect. However, we confirmed the stress enhancement by simulation and the current enhancement by measurement

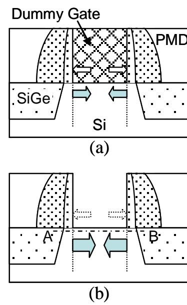


Fig. 1: Concept of stress enhancement (a) before and (b) after dummy gate removal.

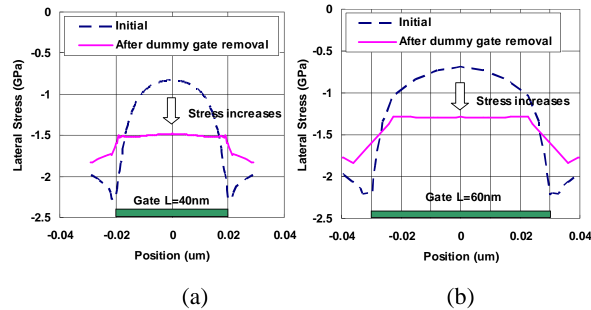


Fig. 2: Lateral stress distribution along A-B of Fig. 1(b). A-B is 1nm below the surface.
(a) L=40nm, (b) L=60nm.

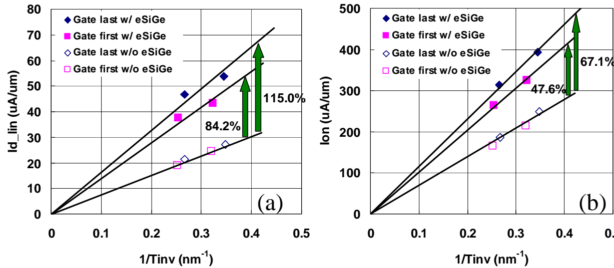


Fig. 3: Id -Tinv^{-1} characteristics for gate first and gate last processes at (a) linear (Vg=-1V, Vd=0.05V) and (b) saturation (Vg=Vd=-1V) regions.

3 New Channel Recess Structure

In addition to the damascene gate process with eSiGe S/D, the effect of channel recess after dummy poly-Si gate removal is also examined in detail. Fig. 4 shows a

conceptual image of the stress enhancement effect of channel recess. The compressive stress above the recessed channel is transferred to the channel, resulting in higher channel stress. Simulation results for different channel recesses are shown in Fig. 5. As seen in the figures, the lateral compressive stress in the channel region is enhanced by the channel recess. Fig. 6 shows recess depth dependence of lateral stress. Channel stress is found to increase up to a recession of about 15 nm. It is also found that the channel stress is more enhanced for shorter Lg, which suggests that channel recession is more effective for scaled devices.
Experimental verification was also performed [4]. A pFET was fabricated based on the damascene process, and a TiN/HfO2 gate stack was used. Channel recession, consisting of plasma oxidation followed by wet etching, was performed after dummy poly-Si and oxide layer removal. TEM images of the device w/ and w/o channel recess are shown in Fig. 7, showing an approximately 2.5nm channel recess. Fig. 8 shows Ion-Ioff characteristics for different devices, proving that a 2.5nm channel recess provides a 14% Ion enhancement at Ioff=100nA/um [4].

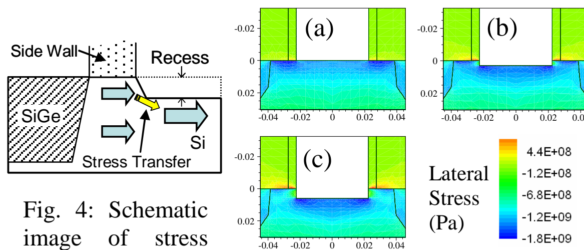


Fig. 4: Schematic image of stress enhancement mechanism with channel recess.

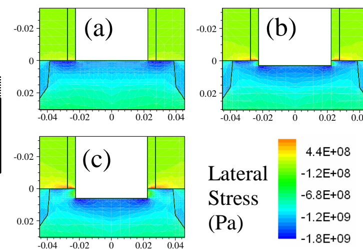


Fig. 5: Stress simulation for various channel recesses: (a) w/o recess, (b) 3nm recess, (c) 6nm recess.

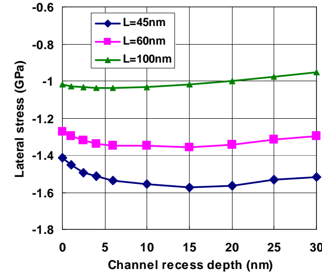


Fig. 6: Recess depth dependence of stress at the channel's center 1nm below the surface.

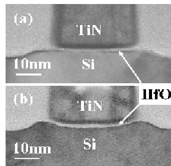


Fig. 7: TEM images of fabricated devices. (a) w/o channel recess, (b) w/ 2.5nm channel recess.

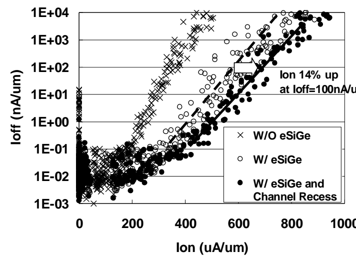


Fig. 8: Ion-Ioff characteristics for w/o eSiGe, w/ eSiGe and w/ eSiGe+channel recess.

4 Effect of Substrate Recess

In reality, the substrate next to the channel is often recessed due to gate etching or side wall formation. In fact, the substrate of the fabricated devices shown in Fig. 7 is recessed approximately 3nm. Fig. 9 shows the effect of substrate recess on the channel stress. The stress to the channel is reduced significantly due to lack of SiGe next to the channel. However, the channel recess moves the channel surface to the region with strong stress and thereby the channel stress increases. Figs. 10 and 11 show the lateral stress distribution with various channel recesses for the substrate recesses of 3nm and 6nm, respectively. In both cases, the stress at the channel is increased as the channel is recessed. Fig. 12 shows recess depth dependence of lateral stress at the channel's center 1nm below the surface for two cases of the substrate recess. As can be clearly seen, the effect of the channel recess is significant for deeper

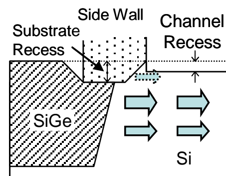


Fig. 9: Effect of substrate recess. The stress at the channel is reduced due to lack of SiGe next to the channel.

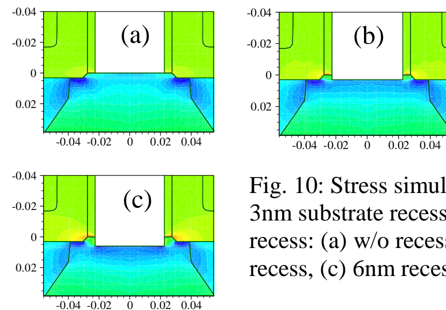


Fig. 10: Stress simulation for 3nm substrate recess. Channel recess: (a) w/o recess, (b) 3nm recess, (c) 6nm recess.

substrate recess. The channel recess process recovers the stress reduction due to the substrate recess, and this effect is noticeable for short gate devices. The proposed channel recess process offers a substantial advantage for fabrication of future scaled pFET devices.

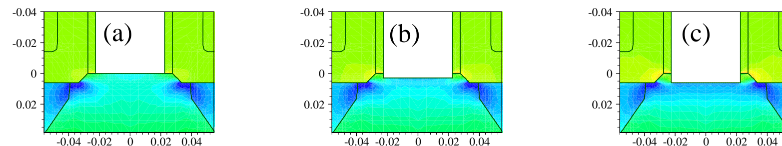
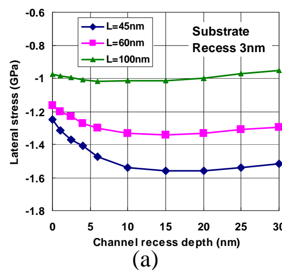
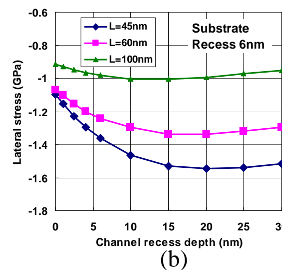


Fig. 11: Stress simulation for 6nm substrate recess. Channel recess: (a) w/o recess, (b) 3nm recess, (c) 6nm recess.



(a)



(b)

Fig. 12: Recess depth dependence of stress at the channel's center for different substrate recesses. ((a) 3nm, (b) 6nm)

5 Summary

The stress enhancement effect based on the damascene gate process with eSiGe S/D was investigated in detail. Through simulations and experiments, we proved that dummy gate removal and channel recession strategies contribute significantly to stress enhancement. The combination of these strategies is a clear advantage of the gate last process and shows great potential for achieving high performance in future scaled pFETs.

References

[1] H.S. Yang et al., IEDM Tech. Dig., p.1075 (2004)
[2] S. Tyagi et al., IEDM Tech. Dig., p.1070 (2005)
[3] Y. Tateshita et al., IEDM Tech. Dig., p.63 (2006)
[4] J. Wang et al., Symp. VLSI Tech., (2007), to be published.
[5] M.S. Lundstrom, IEEE Electron Device Lett., vol.22, p.293 (2001)
[6] C.S. Smith, Phys. Rev., vol.94, p.42 (1954)