Line Edge and Gate Interface Roughness Simulations of Advanced VLSI SOI-MOSFETs

T. Herrmann*, W. Klix*, R. Stenzel*, S. Duenkel*, R. Illgen*, J. Hoentschel°, T. Feudel°, M. Horstmann°

* Dep. of Electr. Eng., Univ. of Appl. Sciences Dresden, 01069 Dresden, Germany
tom.herrmann@et.htw-dresden.de

° AMD Saxony LLC & Co. KG, 01109 Dresden, Germany

Abstract

The influence of line edge and gate interface roughness on SOI-MOSFET performance is studied by simulation. Both types of roughness were implemented in the device simulator SIMBA through the Fourier synthesis approach and the simulations were performed with the drift diffusion and the quantum drift diffusion models. Scaled transistors showed more sensitivity to rough interfaces with shallow junctions.

1 Introduction

For advanced VLSI SOI-MOSFETs where the gate oxide has a physical thickness of 1.3 nm or less, interface roughness variations of up to 50% have a tremendous impact on the electrical performance. A rougher interface reduces the saturation current and degrades the transistor performance. In the device simulator SIMBA integrated roughness models were used to simulate the influence of the interface and line edge roughness (LER) on Poly Si. The models are based on the Fourier synthesis of a Gaussian distributed autocorrelation function. Advanced VLSI SOI-MOSFETs with gate length of 55 nm and below were simulated using the drift diffusion and quantum drift diffusion models.

2 Interface Modeling

The Fourier synthesis approach with a fitted Gaussian distribution of the autocorrelation function is the foundation of the implemented roughness model [1]. The Fourier transformation of the Gaussian distributed autocorrelation function leads to the power density spectrum of the interface roughness. Hence, the amplitude spectrum could be calculated. Inverse Fourier transformation of the amplitude spectrum including a random phase generates a stochastic roughness function with power density equal to the measured surface. The quantized roughness function is applied to the gate oxide/silicon film interface (Fig. 1), where the parameters for varying the roughness function are the root mean square (rms) and the correlation length (corl). The LER modeling approach is similar but with different implementation. In SIMBA, the halo implantations and the extension implantations are shifted by the roughness function, varying the metallurgical channel length (Fig. 2).

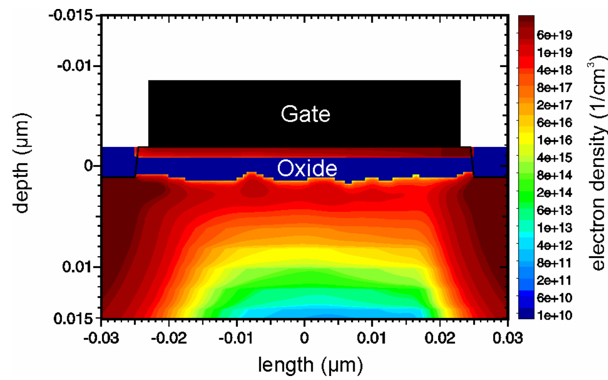

Figure 1: Carrier concentration at the rough interface using the quantum drift diffusion model.

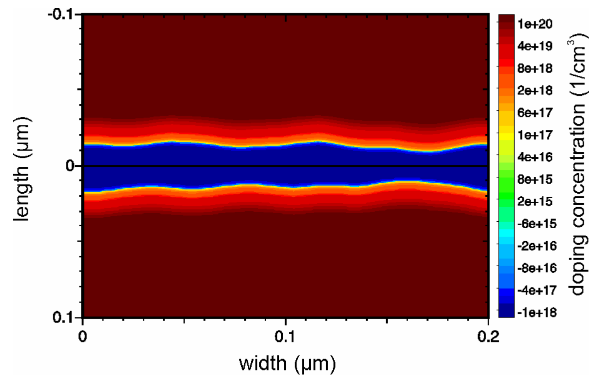

Figure 2: Doping concentration with line edge roughness.

3 Simulation Results

Simulations on SOI-MOSFETs were performed with a correlation length of 3nm, 2nm gate oxide and 55nm gate length. Using the drift diffusion model, simulations show a 31% increase in saturation current and a larger standard deviation when decreasing the rms value of the Gaussian distribution from 0.3nm to 0.1nm. Comparatively, simulations using the quantum drift diffusion model demonstrate an 11% increase in drain current. Quantum confinement of the inversion charge carriers pushes the maximum of their distribution away from the interface leading to less influence of roughness on carrier mobility. A scaled transistor with 1.2 nm gate oxide, 30 nm gate length and shallow extension areas show a stronger impact on decreasing gate interface roughness (Fig. 4); this results in a current increase of ~24%. In comparison with the previously simulated device described above, the inversion charge carrier maximum is higher and closer to the interface due to the reduced gate oxide thickness. The influence of the gate interface roughness on the carriers is therefore higher.

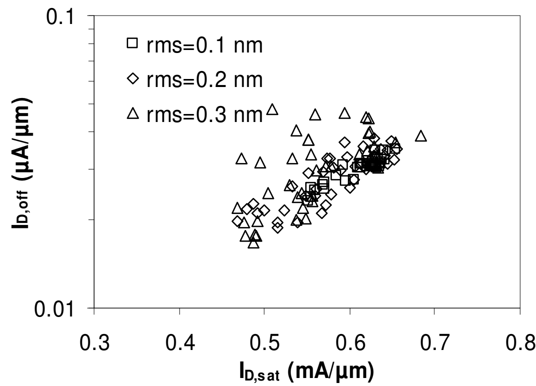

Figure 3: Standard transistor with gate interface roughness.

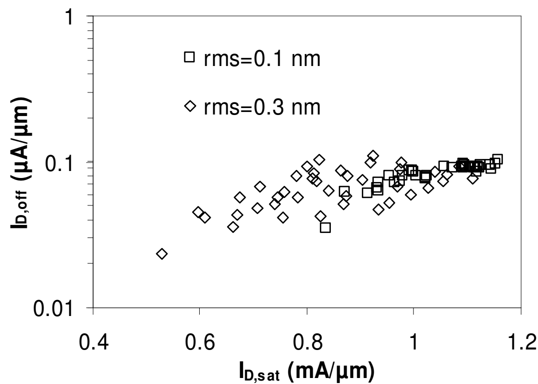

Figure 4: Scaled Transistor with gate interface roughness.

Three dimensional devices were simulated using the drift diffusion model, with a device width of 200 nm and LER correlation length of 20 nm. Variations of the electrical transistor parameters based on LER become important with gate length shrinking, where LER predominately influences the leakage current of the MOSFETs. With a 55nm device, leakage current and standard deviation increases as a function of rms. A 17% increase in leakage current is observed when increasing the rms from 1nm to 2nm. The leakage current is amplified to 39% when incrementing to 3 nm rms (Fig 5). Advanced channel doping profiles reduce this influence slightly but transistor scaling to 30 nm gate length increases the leakage current difference up to 50% between 1 nm and 2 nm rms and nearly another 100% with an rms of 3nm (Fig 6). Short channel effects are apparent when the metallurgical channel length varies across the device. The overall leakage current increases due to the nonlinear behavior at channel length variation [2].

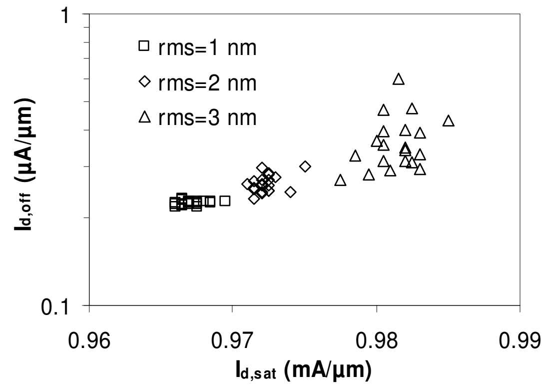

Figure 5: Standard transistor with line edge roughness.

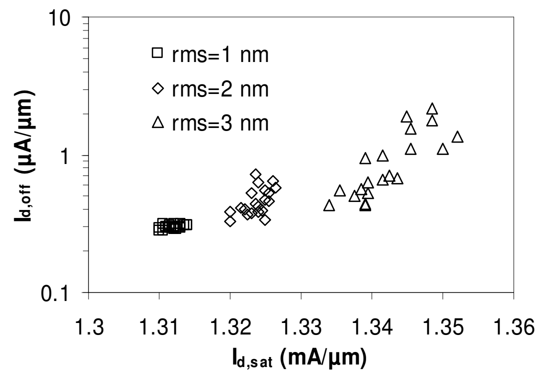

Figure 6: Scaled transistor with line edge roughness.

Acknowledgements

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