SIMULATION OF SEMICONDUCTOR PROCESSES AND DEVICES Vol. 12
Edited by T. Grasser and S. Selberherr - September 2007

Thin Body Effects to Suppress Random Dopant Fluctuations in Nano-Scaled MOSFETs

Y. Ashizawa and H. Oka

Fujitsu Laboratories Ltd., 50 Fuchigami, Akiruno, Tokyo, 197-0833, Japan
ashizawa.yoshio@jp.fujitsu.com

Abstract

The intrinsic parameter fluctuations induced by random discrete dopants (RDD) in nano-scaled MOSFETs are studied by applying the quantum mechanical approach. The increase of effective oxide thickness (EOT) by the quantum mechanical corrections generally makes gate controllability worse. However, as far as ultra thin body (UTB) devices, the increase of EOT improves gate controllability by suppressing leakage current because it reduces electrical body thickness by the constraint of the physical body thickness.

1 Introduction

Nano-scaled MOSFETs with doped channels are carefully investigated with statistical simulations. Considering the quantum mechanical corrections, scaling would be encouraged by making use of a specific range of body thickness which is originally insensitive to threshold voltage fluctuations.

2 The Simulation Approach

The quantum mechanical approach is proposed to describe the mobile carrier trapping around individual discrete dopants because the classical approach suffers from strong mesh space dependence in atomistic simulations [1]. This approach certainly gives consistent device characteristics with that of continuous doping. This work is carried out with a 3-D drift-diffusion (DD) device simulator [2]. The quantum mechanical corrections around RDD are included by adopting the density gradient (DG) method in the device simulator.

3 Discussion

Fig. 1 illustrates single gate SOI device structures to compare the effect of atomistic doping profiles. Cont is a structure with continuous doping. CIC represents the numerical technique of Cloud In Cell, which is commonly used in numerical discretizations. CIC-Full is atomistically doped one, and CIC-Ch is one doped atomistically in the channel but continuously in the SD regions to avoid gate length fluctuations.
Fig. 2 compares threshold voltage distributions. Straight relationship means normal distribution and the slope represents the inverse of σV_{th}. The threshold voltage crossing at 0 on y-axis is the average for each method. The difference in the average is caused by numerical modeling because the physical proposition is the same. It

should be noted that threshold voltages for CIC-Full and CIC-Ch by the DG approach are consistent with that of Cont-DG. This makes sure of the validity of the quantum mechanical approach.

SG nMOSFET	Cont	CIC-Ch	CIC-Full
Bird's-eye View of Doping Profiles			
$L/W/T_{ox}/T_{Si}$(nm)	10/10/0.5/4	10/10/0.5/4	10/10/0.5/4
Channel $N_a=10^{19}cm^{-3}$	Continuous	Atomistic	Atomistic
SD $N_d=5x10^{19}cm^{-3}$	Continuous	Continuous	Atomistic
Metallurgical Gate Length	Exactly 10 nm Abrupt SD Profiles	10 nm Abrupt SD Profiles	10+ nm Fluctuated Lg

Figure 1: Single gate SOI device structures with different doping profiles.

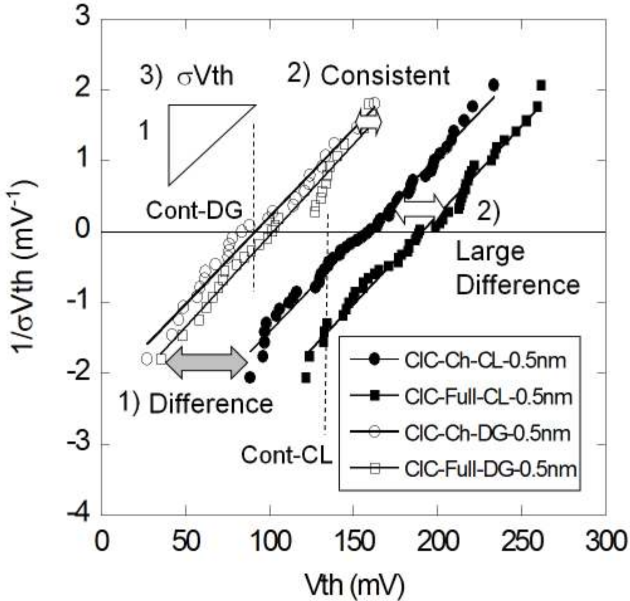

Figure 2: Normal probability plots of V_{th} for the classical approach and the DG approach.

There can be seen three distinct features.
1) Difference in V_{th} between the classical approach and the DG approach.
2) Difference in V_{th} between CIC-Full and CIC-Ch doping profiles for each approach.
3) Nearly the same slope for all methods.

The first one is caused by poor gate controllability due to the significant increase of EOT or the increase in resistance due to strong mobile charge trapping in the classical model.
The second one is caused by the evaluation of electrical gate length. Fig. 3 (a) shows a bird's-eye view of atomistic dopant distribution. Fig. 3 (b) shows the net doping profile at the middle. In Fig 3 (c), because the mobile charge is loosely trapped by discrete quantum potential wells, the electrical gate length is smeared at 10 nm. This is the reason why the V_{th} distribution of CIC-Full is consistent with that of CIC-Ch. In Fig. 3 (d), because the mobile charge is sharply trapped at dopant positions, the electrical gate length is reflected by the net doping profiles. Consequently, it makes the difference in V_{th} between CIC-Full and CIC-Ch doping profiles. It is suggested that the electrical gate length be more moderately varied than metallurgical one by the pure classical model.

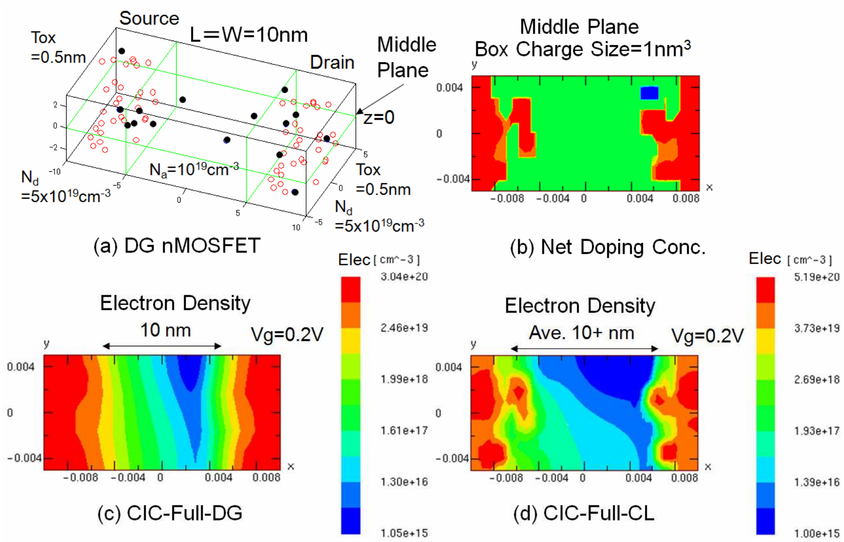

Figure 3: (a) Bird's-eye view of a double gate device structure with atomistic doping. (b) Net doping concentration at the middle plane. Comparison of electron density distributions for the DG approach (c) and the classical approach (d).

The third one comes from the thin body effect that the increase of EOT by the quantum mechanical corrections reduces the effective body thickness due to the constraint of the physical body thickness. This goes against the general understanding that σV_{th} is proportional to EOT in bulk structures [3].
Classical model is helpful to understand the reason why there is little difference in σV_{th} (the inverse of the slope in Fig. 2). The dark space is introduced to understand the quantum mechanical corrections, which is assumed to be an oxide layer whose permittivity is that of pure silicon as shown in Fig. 4 (a). The rest of the body is white space. Fig. 4 (b) shows the analytical response surface of σV_{th} [4]. It attains the maximum of σV_{th} along T_d = 0, but σV_{th} is insensitive around the vicinity of peak electron density distributions due to the quantum mechanical corrections. It can be

qualitatively seen that UTB devices are insensitive to the minute variations of T_d induced by RDD.

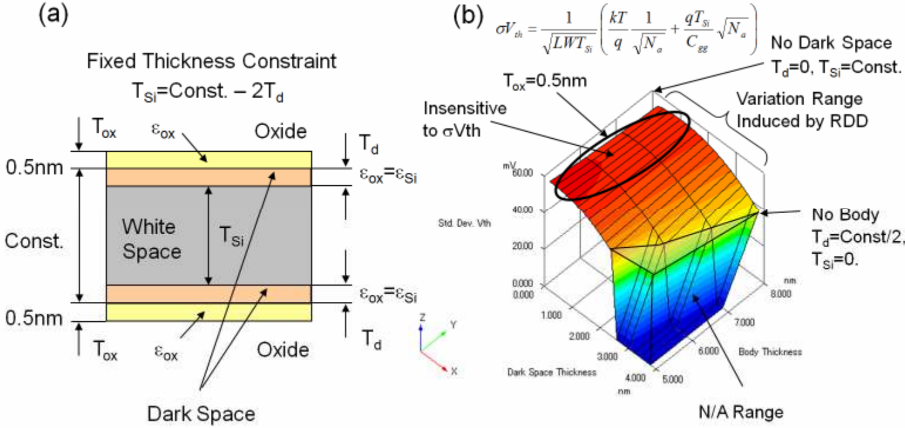

Figure 4: (a) Schematic view of the dark space approximation. (b) The response surface of σV_{th} as a function of dark space thickness T_d and body thickness *Const.*

4 Conclusion

Considering the quantum mechanical corrections, the increase of EOT generally makes gate controllability worse. However, as far as UTB devices, it overcomes poor gate controllability by suppressing leakage current because it reduces the white space thickness within the substrate. The UTB MOSFET structure with doped channels is one of the promising device structures for the future scaling because it is robust against RDD.

Acknowledgements

The authors wish to thank Prof. A. Asenov, Dr. G. Roy, Dr. A. R. Brown, and everyone else in the device modeling group of the University of Glasgow, U.K. for fruitful discussions.

References

[1] G. Roy, A. R. Brown, F. Adamu-Lema, S. Roy, and A. Asenov, "Simulation Study of Individual and Combined Sources of Intrinsic Parameter Fluctuations in Conventional Nano-MOSFETs", IEEE Trans. Electron Devices, vol. 53, no. 12, pp. 3063-3069, 2006.

[2] http://www.selete.co.jp/?lang=EN, Unpublished.

[3] T. Mizuno and A. Toriumi, "Experimental Study of Threshold Voltage Fluctuation Due to Statistical Variation of Channel Dopant Number in MOSFET's", IEEE Trans. Electron Devices, vol. 41, no. 11, pp. 2216-2221, 1994.

[4] T. Mizuno, "New Channel Engineering for Sub-100 nm MOS Devices Considering Both Carrier Velocity Overshoot and Statistical Performance Fluctuations", IEEE Trans. Electron Devices, vol. 47, no. 4, pp. 756-761, 2000.