

Physics-Based Simulation of $1/f$ Noise in MOSFETs under Large-Signal Operation

Sung-Min Hong*, Hong-Hyun Park*, Chan Hyeong Park[†], Myoung Jin Lee*,
Hong Shick Min*, and Young June Park*

*School of EECS and NSI-NCRC, Seoul National University, Seoul 151-744, Korea
hi2ska2@isis.snu.ac.kr

[†]Dept. of Electronics and Commu. Eng., Kwangwoon Univ., Seoul 139-701, Korea
chanpark@kw.ac.kr

Abstract

$1/f$ noise in MOSFETs under large-signal excitation, which is important in CMOS analog and RF circuits, is modeled as a perturbation in the semiconductor equations employing the oxide-trapping model. The oxide-trapping model for a MOSFET in periodic large-signal operation shows that $1/f$ noise reduces more than the small-signal noise model predicts as the gate OFF voltage decreases further below the threshold voltage.

1 Introduction

Experimental results for the drain $1/f$ noise current under the large-signal operation show that the power spectral density of the drain $1/f$ noise current is much lower than the estimate using the small signal $1/f$ noise model [1]. In this paper, we present a numerical framework, which is based on the CLESICO system [2], to model and simulate the $1/f$ noise under the large-signal as well as small-signal operation regimes.

2 Oxide-Trapping Model

Figure 1 shows the energy band diagram that illustrates the possible carrier transition processes at the interface and in the oxide, considered in this paper. Electrons in the conduction band can get trapped (process a) or de-trapped (process b) from the localized defect centers at the interface. The trapped electrons can also communicate with defect centers that have the same energy in the oxide through tunneling (processes c and d).

Let us consider an oxide trap level with energy E_t , whose volume density is $N_{t,ox}$. $N_{t,int}$ denotes the sheet density of the interface traps which can interact with the oxide trap with energy E_t . Also $n_{t,ox}$ and $n_{t,int}$ represent the trapped electron volume density in the oxide trap and the trapped electron sheet density in the interface trap, respectively. The expressions characterizing the processes a, b, c, and d in Fig. 1 then become

$$r_{n,int} = c_n n (N_{t,int} - n_{t,int}), \quad (1)$$

$$g_{n,int} = c_n n_{t,int} n_1, \quad (2)$$

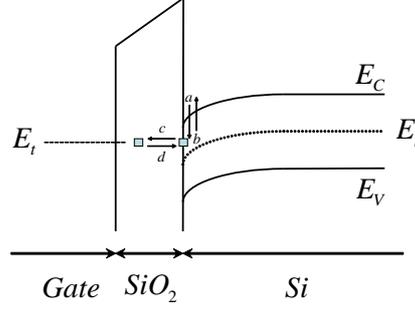


Figure 1: Energy band diagram that illustrates the possible carrier transition processes at the interface and in the oxide. Only the traps with energy E_t are depicted.

$$r_{int,ox} = T n_{t,int} \Delta x (N_{t,ox} - n_{t,ox}), \quad (3)$$

$$g_{int,ox} = T (N_{t,int} - n_{t,int}) n_{t,ox} \Delta x, \quad (4)$$

respectively. Note that $r_{n,int}$, $g_{n,int}$, $r_{int,ox}$, and $g_{int,ox}$ have the units of $\text{cm}^{-2} \text{sec}^{-1}$. In Eqs. (1)–(4), n is the electron volume density in the conduction band at the interface, c_n is the capture coefficient of electrons, n_1 is the Shockley density which is the electron density when the electron quasi-Fermi energy is equal to E_t , T is the tunneling coefficient with the units of $\text{cm}^2 \text{sec}^{-1}$, and Δx is the vertical length of the control volume for the oxide trap. The tunneling coefficient is calculated using the trapezoidal approximation. Now the electron continuity equation, the interface trap continuity equation, and the oxide trap continuity equation can be written as

$$\int_{V_{int}} d^3 r \left(\nabla \cdot \mathbf{J}_n - q \frac{\partial}{\partial t} n \right) = q \int_{A_{int}} da (r_{n,int} - g_{n,int}), \quad (5)$$

$$0 = q \int_{A_{int}} da \left(\frac{\partial}{\partial t} n_{t,int} - r_{n,int} + g_{n,int} + r_{int,ox} - g_{int,ox} \right), \quad (6)$$

$$0 = q \int_{V_{ox}} d^3 r \frac{\partial}{\partial t} n_{t,ox} + q \int_{A_{int}} da (-r_{int,ox} + g_{int,ox}), \quad (7)$$

respectively. In Eqs. (5)–(7), V_{int} is the control volume whose surface includes the interface, A_{int} is the interface, and V_{ox} is the control volume of the oxide node where the oxide trap is located.

Since the trap centers at the interface and in the oxide are distributed in energy and space, discretization in both variables is needed. In Ref. [3], Hou *et al.* discretized only the trap levels at the electron quasi-Fermi energy, mainly due to the computational efficiency. This approach can be valid only when the electron quasi-Fermi energy of the oxide trap is aligned with that of the interface trap. However, when the MOSFET is switched periodically, the validity of this assumption is in doubt, because the electron trapping and de-trapping by the oxide traps, which are related to $1/f$ noise in the

oxide-trapping model, are known to be slow processes. Therefore, in this paper, we discretize the selected energy range in the oxide bandgap in small discrete energy interval ΔE_i . Although this implementation is computationally expensive, we expect that it gives more accurate results. Instead, we make a simplifying assumption to reduce the computational complexity, i.e. the quasi-static approximation for the (fast) interface traps [3, 4]. Since we calculate the self-consistent solution of Poisson's equation and the continuity equations, the Poisson effect of the trapped electron in the oxide trap is automatically included in our simulation.

3 Simulation Results

We calculate the power spectral density of the drain noise current when the MOSFET is in a large-signal operation. We consider a periodically-switched MOSFET, whose gate length is $2.0 \mu\text{m}$. The thickness of the gate oxide is 9.0 nm . Since our aim is to simulate the experimental set-up given in [1], the gate bias voltage is driven by a square-wave signal with 50 % duty cycle and of 10 kHz frequency. The ON voltage is fixed to be 1.0 V . The harmonic balance simulation for the periodic steady-state is carried out including 12 harmonics plus DC, leading to 25 collocation points. In this case, the small-signal noise model predicts a noise power reduction by 6 dB.

Figure 2(a) shows the simulated power spectral densities of the drain $1/f$ noise currents as a function of frequency for four OFF gate voltages of 0.5 V , 0.4 V , 0.3 V , and 0.1 V where the threshold voltage is 0.5 V . To further analyze the $1/f$ noise dependence on the OFF voltage levels, a noise reduction factor for different OFF voltages is plotted in Fig. 2(b). Additional noise reduction over 6 dB is observed for lower OFF voltages.

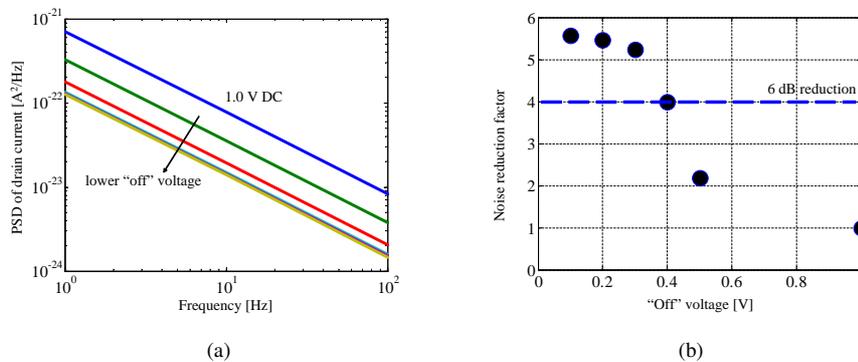


Figure 2: (a) Simulated power spectral densities of the drain $1/f$ noise currents. (b) Noise reduction factor. The drain bias voltage is 10 mV .

The conversion Green's function (from baseband to baseband) for the oxide trap continuity equation is shown for the OFF voltage of 0.1 V in Fig. 3(a). It is almost half of the corresponding Green's function for the DC 1.0 V case. It means that 6 dB noise reduction is merely due to the reduced transfer function. Figure 3(b) shows the oxide trap occupancy during the OFF cycle for the OFF voltage of 0.1 V . The trapped elec-

tron density in the oxide trap is reduced, for the lower OFF voltages, whence the power spectral density of the Langevin noise source is also reduced. Therefore, additional noise reduction over 6 dB is due to the reduced trap occupancy.

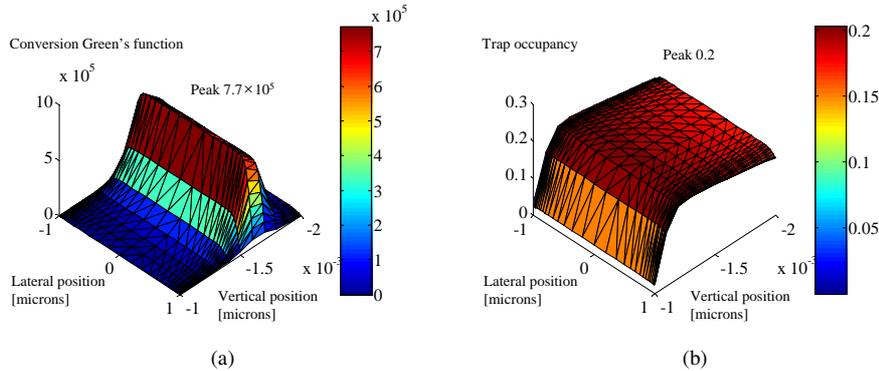


Figure 3: (a) Real part of the conversion Green's function (from baseband to baseband) for the oxide trap continuity equation. (b) Oxide trap occupancy during the OFF cycle. The gate contact is located from $-1.0 \mu\text{m}$ to $1.0 \mu\text{m}$ in the lateral position. The zero point in the vertical position is the oxide-silicon interface. The OFF voltage is 0.1 V .

4 Conclusion

$1/f$ noise in MOSFET in large-signal operation was modeled using the oxide-trapping model. In this model, additional noise reduction over 6 dB was observed for the low OFF voltages. Additional noise reduction over 6 dB is due to the reduction of the oxide trap occupancy.

Acknowledgements

This work was supported by the NCRC program of the KOSEF through the NSI at Seoul National University and by Samsung Electronics Company (0414-20050009 and 0414-20050037). C. H. Park's work has been supported by Nano IP/SoC Promotion Group of Seoul R&BD Program in 2007, by Hynix Semi. Inc. and by the MIC, Korea under ITRC support program supervised by the IITA (IITA-2006-(C1090-0603-0008)).

References

- [1] A. P. van der Wel, et al., *IEEE Electron Device Lett.*, vol. 21, pp. 43–46, 2000.
- [2] S.-M. Hong, et al., *International Conference on Simulation of Semiconductor Processes and Devices*, 2005, pp. 119–122.
- [3] F.-C. Hou, et al., *IEEE Trans. Electron Devices*, vol. 50, pp. 846–852, 2003.
- [4] H. Nah, et al., *International Conference on Simulation of Semiconductor Processes and Devices*, 2003, pp. 75–78.