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Upcoming Challenges for Process Modeling

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Abstract

In industrial environments, numerical simulation has become an indispensable tool for the development and optimization of especially front-end processes. In order to remain useful for future technology nodes, process simulation has to follow and partly even anticipate paradigm shifts of state-of-the-art processes and new materials for future nanoelectronic devices. Within this article, the author presents his personal view of unsolved and upcoming issues that have to be addressed and solved in future.

1 Introduction

According to a famous quote attributed to a variety of persons from Yogi Berra to Niels Bohr [1], prediction is very difficult, especially about the future. For semiconductor devices, modern augury has been assisted especially by the Technology Roadmaps for Semiconductors (ITRS) [2] and its predecessors, the National Technology Roadmaps for Semiconductors (NTRS), which have been predicting and driving the pace of semiconductor technology at the same time. One of the most important self-fulfilling prophecies of the ITRS, noted already by Gordon Moore in 1965 [3], is the hitherto unbroken miniaturization of electron devices. In this development, Technology Computed Aided Design (TCAD) is a main tool which has the potential to reduce development costs by as much as 40% "if appropriately used" [2].
Future requirements on TCAD can not only be found in the Modeling and Simulation Section of the ITRS. Within Europe, the industrial User Groups UPPER (User Group for Process Simulation European Research), UPPER+ (User Group for Process Simulation European Research + Device Simulation) [4], and SUGERT (Strategic User Group for European Research on TCAD) [5] were collecting and publishing detailed and prioritized specifications to stimulate the required research activities. Comparing ITRS and the SUGERT specifications, which are accessible at least to registered users, the latter are significantly more detailed. In fact, the two specifications are meant to complement each other with the SUGERT consortium forming the European part of the International Technology Working Group (ITWG) of the Modeling and Simulation Section of the ITRS. In addition to having been serving as Specifications Secretary in these projects, the author has been benefiting from organizing the major European front-end process simulation projects FRENDTECH (Front-End Models for Silicon Future Technology) [6] and ATOMICS (Advanced Front-End Technology Modeling for Ultimate Integrated Circuits) [7]. Within the chain of TCAD from crystal growth up to circuits,

the simulation of the effects of front-end process steps on the distribution of dopants and on the topography of devices is usually the first step. The remainder of this article emphasizes some issues associated with the formation of the shallow *pn* junctions by ion implantation and annealing that seem particularly important to the author.

2 Requirements from Doping Technologies

Until about the 90 nm technology node in 2004, device scaling was based primarily on the reduction of gate length and oxide thickness. Modeling of front-end processes has been facing challenges caused by a continuous reduction of the implant energies and of the thermal budgets of the annealing schemes from soak anneals to the spike anneals which are now used for production. From the point of view of process simulation, transient phenomena in diffusion and activation especially of boron were for long the main issue. Although these effects are qualitatively understood, their quantitative modeling is still a problem. Another issue is that the best models available are usually too complicated and too slow to be used in multi-dimensional process simulation, so that often compromises have to be found. For future technology nodes, the need to minimize dopant diffusion and to maximize electrical activation will require low-temperature solid-phase epitaxy or millisecond annealing schemes in addition to point-defect engineering methods. To increase the drive current by 17% per year as predicted by the ITRS for high-performance logic devices, strain was used from 2004 on to enhance the channel mobility [8]. This required the use of silicon-germanium alloys. Other device concepts were based on silicon-on-insulator and silicon-on-nothing structures. All these processing conditions and materials have to be included in process simulation in maintain its usefulness for future technology nodes.
Considering the diverse requirements, it is only natural to ask for the level of confidence at which process simulation is useful for process development. In fact, there are generally delays between the first suggestion of a technological concept, the qualitative understanding of its effects, and finally the quantitative reproduction within TCAD. This problem was summarized concisely by Mark Law by the aphorism “modeling tomorrow yesterday’s technology” [9]. On the other hand, process simulation is especially helpful in the initial phase of technology development for the preselection of technological options. In this stage, models often contain heuristic components, and the correct prediction of trends is more an issue than absolute accuracy. Later, for the optimization of designs, accuracy and speed are important.

3 Stress and Strain Effects

As mentioned in the introduction, strain was implemented intentionally as a mobility booster in devices that went into production in 2004. Already long before, diffusion phenomena were associated with stress. However, such phenomena have not been fully understood and have been largely ignored in the development of front-end models as well as in process simulation. In any case, their quantitative understanding and a clear separation from other effects may be important for future technology nodes.
Besides the salient effects on the charge carrier mobilities, stress affects the width of the band gap and has widespread direct and indirect effects on the defects in a semiconduc-

tor, and among them in particular on dopants. One of the first evidences of such effects was reported by Todokoro and Teramoto [10]. They observed an enhanced diffusion of boron in silicon below a mask window of a deposited oxide layer which reduced with the distance from the window edge. The effect was attributed to laterally inhomogeneous tensile stress in the silicon induced by the oxide mask and is a prominent example for one of the major sources of stress, namely strained covering layers. The strain from deposited layers results from the intrinsic film stress and from different thermal expansion coefficients between film and substrate. Similar effects can be expected near locally oxidized structures. Conversely, retarded diffusion of boron was observed below nitride films with the work of Osada et al. [11] as a representative example. Similar effects were observed already before by Mizuo et al. [12] and others during thermal nitridation of silicon. The only problem for associating the latter with stress effects is that nitride growth stops at a thickness of a few nanometers. It is hard to conceive how such a thin layer may introduce stresses of several hundred MPa into the silicon needed to cause stress effects. A second major source of stress arises from impurities that occupy different atomic volumes than silicon atoms. Following Vegard's law, the host lattice constant increases or decreases then within a wide range of concentrations linearly with the local concentration of the impurities. For boron, the strain introduced at a concentration of 2×10^{20} cm^{-3} is about -10^{-3}. A similar contraction would require a hydrostatic pressure of approximately 260 MPa. The local lattice distortions affect already microscopic diffusion processes in their vicinity. Macroscopic diffusion effects can be expected when adjacent regions have different lattice constants. A typical example with germanium as impurity are SiGe buffer layers or SiGe regions grown by selective epitaxy that are used to induce strain into the channels of MOS transistors. A second example are highly doped regions like drain and source regions in CMOS, or emitters in bipolar technologies. While strain effects in the former systems have been studied intensively using strained and strain-relaxed SiGe layers [13], strain effects in the latter have traditionally been ignored and lumped into diffusion effects.

At this point it is necessary to shortly summarize the expected effects of stress on defects. From thermodynamic considerations, their concentrations under a non-negligible stress σ is expected to change in proportion to $\exp(\sigma\Delta V^f/kT)$ with ΔV^f being the respective formation volume. For self-interstitials and other interstitial defects, the concentration is expected to increase under compression and to decrease under tensile conditions. For vacancies and vacancy-related defects, the situation is less clear because of major relaxations. For some defects, the equilibrium configuration may differ from the unstrained case and the concentrations of charged defects will change with the stress-induced modifications of band structure. Stress may also influence the achievable solubilities of dopants. Bennett et al. [14] recently reported a significantly enhanced activation of antimony in tensile-strained silicon while arsenic was not affected. Considering diffusion, it can be expected that all saddle-point energies may be affected. Stress gradients are also driving forces for the redistribution of defects, including intrinsic point defects and dopants. Such effects are well established, e.g. in electromigration, but have rarely been included in diffusion models for silicon. Considering that impurities at high concentrations induce stress and that stress gradients drive their redistribution, a parallel mechanism to Fick's laws is established that comprises non-local effects [15].

4 Annealing Strategies and Point-Defect Engineering

With the continuously decreasing feature sizes of devices, activation of dopants, if possible even beyond the maximum solid solubility, with a minimum of diffusion is a primary goal. Therefore, the spike annealing techniques currently in use in production are soon expected to be replaced or complemented by annealing strategies with significantly smaller thermal budgets and, especially for boron, complemented by point-defect engineering techniques to further reduce dopant redistribution and enhance their activation.

One of the primary alternatives investigated in the recent past is preamorphization in combination with solid-phase-epitaxial regrowth (SPER). During SPER at low temperatures, boron is activated up to a concentration of 3×10^{20} cm^{-3} [16]. A potential disadvantage of the method is that the end-of-range disorder is not annealed and the self-interstitials bound in them may lead to an enhanced deactivation during subsequent process steps at elevated temperatures. To prevent such a deactivation, carbon and fluorine are co-implanted into the preamorphized areas. The effects of both are pretty well understood. Carbon is introduced at substitutional sites during SPER and acts later as an efficient trap for self-interstitials by forming a variety of carbon-self-interstitial complexes [17]. For fluorine, the situation is somewhat more complex. According to the work of Diebel et al. [18] and Impellizzeri et al. [19], fluorine is introduced in the form of fluorine-vacancy complexes during SPER which later trap the self-interstitials arriving from the end-of-range disorder. Although a qualitative understanding has been achieved, no implementation of the conclusions into commercial process simulation software is available.

A viable alternative to SPER are millisecond annealing strategies like flash-assisted RTP or non-melt laser annealing with peak temperatures in the range from 1100 to 1300 °C. Their advantage is clearly that the thermal budget suffices to remove the implantation damage while dopant redistribution is minimal [20]. Although first attempts to simulate the effects of flash-assisted RTP were successful [21], this cannot be generalized since the processing time may be shorter than the time constant of some defect reactions. The simulation of other millisecond annealing strategies may suffer in addition from the lack of precise data about the temperature during annealing.

In order to increase solubility and to further decrease diffusion, annealing schemes for implants into crystalline silicon can be combined with high-energy implants to introduce vacancies into the near-surface regions. This option is especially effective for silicon-on-insulator technologies for which the self-interstitial-rich part of the high-energy implanted profile can be pushed beyond the top silicon layer. Venezia et al. [22] named this process “vacancy implantation” and demonstrated that it may suppress transient enhanced diffusion. Recently, Smith et al. [23] showed that such a process may also increase the electrical activity of boron-implanted layers. Unfortunately, simulation of such processes is not really advanced. In the end it will may require a full description of vacancy agglomeration in addition to self-interstitial agglomeration, and of vacancy interactions with boron-interstitial clusters.

A possible alternative to thermal annealing is athermal annealing by laser irradiation [24, 25]. Work to understand and model such annealing schemes has probably not even started.

5 New Materials

One of the biggest challenges for process modeling is the introduction of new materials into technology. A typical example for a material that might become important in the future is germanium. Although germanium was used for the first semiconductor devices, it was soon replaced by silicon as the primary semiconductor material. The main reason for this was that germanium has an unstable and non-adherent oxide while that of silicon turned out to be an exceptionally well-suited insulator even down to thicknesses of the order of one nanometer. However, tunneling of charge carriers through the oxide increases dramatically for thicknesses around one nanometer so that gate leakage currents and the standby power of devices become far too high to suggest that much further scaling can be achieved by reducing it. As a remedy, high-κ dielectrics have been suggested which allow the physical thickness to be increased while maintaining the electrical properties. This means, on the other hand, that the primary argument for silicon in the past, its stable oxide, is no longer valid per se.

Comparing the other properties of germanium and silicon shows that germanium has a number of potential advantages which makes it an option for future device technologies: germanium has a four times higher low-field hole mobility than silicon or gallium arsenide. The lower band gap of germanium (0.66 eV) in comparison to silicon (1.12 eV) is a major concern for leakage currents but should allow further scaling of the supply voltage. Preliminary information about the solubilities in germanium [26] indicate that gallium and aluminium can be activated in equilibrium to a concentration of 5×10^{20} cm^{-3}, which is significantly higher than what can be achieved with many tricks for p-type dopants in silicon. Preliminary information about the diffusivities of p type dopants in germanium [27, 28] indicate that all p-type dopants, in particular boron, diffuse slower in germanium than in silicon at a given homologous temperature, i.e. ratio of absolute temperature to absolute melting temperature. Annealing of germanium is expected to require process temperatures of less than 600 °C which makes the material significantly better suited for integration with high-κ dielectrics and metal gates than silicon which requires much higher thermal budgets. Finally, germanium can be integrated without major problems into the current semiconductor production.

The problem for process simulation is now that research on germanium stopped more than forty years ago, and only insufficient information is available on the formation of junctions by ion implantation. Only in the last few years, interest in germanium saw a renaissance which led to a dedicated symposium at the 2006 Spring Meeting of the European Materials Research Society which received significant attention [29]. Research in silicon during the time germanium was set aside has lead to a comprehensive description of diffusion and activation during equilibrium and non-equilibrium situations. There exist largely reliable data sets about the diffusion of dopants [30], including their Fermi-level dependences and diffusion mechanisms, i.e. whether they diffuse via an interaction with self-interstitials or vacancies. Transient diffusion phenomena have been explained by the Ostwald ripening of self-interstitial agglomerates [31] which result from the implantation damage, and transient clustering by the formation of complexes which comprise dopant atoms and intrinsic point defects.

In germanium, the situation is most drastically explained by the reported diffusion coefficients of boron. Until 2004, only two sets of experiments were known from Dunlap

[32] and Meer and Pommerrenig [33] that disagreed by roughly two orders of magnitude. Within the European project FRENDTECH, Uppal et al. [28] investigated boron diffusion in germanium as one end point of Si_xGe_{1-x} alloys. The surprise was quite large when it was clear that the real diffusion coefficients are again more than two orders of magnitude smaller than the smallest values before. The small diffusion coefficient was suggested to reflect diffusion via self-interstitials. Diffusion of other dopants as well as self-diffusion are believed to involve predominantly a vacancy mechanism although no conclusive experiment has been performed up to now. For arsenic, as an example, Vainonen-Ahlgren et al. [34] and Bracht and Brotzmann [35] interpreted their diffusion experiments in terms of a vacancy mechanism. Mitha et al. [36], on the other hand, had suggested before that measurements of the activation volume of arsenic diffusion in germanium are not in agreement with expectations for a simple vacancy mechanism. With respect to implantation damage, the knowledge is similarly rudimentary. Hickey et al. [37] recently reported very instable implantation-induced defects which dissolved much faster in germanium as compared to silicon. Implantation damage was also shown by Satta et al. [38] to be responsible for part of the leakage current of germanium *pn* junctions.
In summary, it will be a challenge to collect all the necessary information needed for predictive process modeling in time should germanium become an alternative to silicon in future technology nodes.

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