Modeling of Re-Sputtering Induced Bridge of Tungsten Bit-Lines for NAND Flash Memory Cell with 37nm Node Technology

Byungjoon Hwang, Yero Lee[1], Jeong-Guk Min[1], Hwakyung Shin, Namsu Lim, Sungjin Kim[1], Won-Young Chung[1], Tai-Kyung Kim[1], Jang-Ho Park, Yun-Kyoung Lee, Donghwa Kwak, Jaekwan Park and Won-Seong Lee

Advanced Technology Development Team, CAE Team[1]
Semiconductor R&D Center, Memory Business, Samsung Electronics Co., Ltd.
San #24, Nongseo-Dong, Kiheung-Gu, Yongin-City, Kyungki-Do, Korea, 449-711
fuzzycom.hwang@samsung.com

Abstract

As the design rule is scaled down, the electrical isolation of metal lines becomes critical. In a high density flash memory with 37nm (pitch=74nm) technology, the threshold voltage shift of ~0.3V is found to be caused by tungsten micro-bridge between adjacent bit-lines. Simulations and experimental data showed that tungsten re-sputtering is occurred during the deposition of HDP (High Density Plasma)-SiO_2 used as the filling dielectric between tungsten bit-lines. In this paper, the model for the tungsten re-sputtering is presented. The plasma simulations are performed to investigate the effects of process factors of HDP-SiO_2 deposition on the formation of micro-bridge using in-house tool, PIE simulator.

1 Introduction

The threshold voltage distribution of about 1V or less should be obtained after programming in the MLC (Multi level Cell) flash devices with 37nm technology [1][2]. Recently, a few random bits, whose threshold voltages are about 0.3V higher

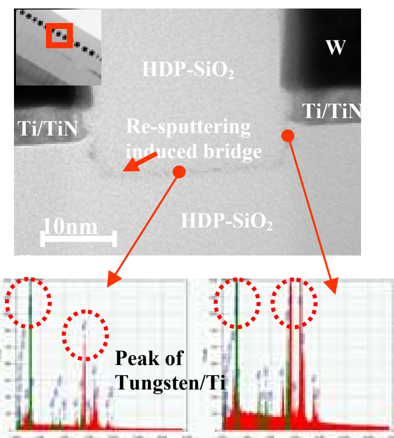

Figure 1: TEM image of tungsten bit-lines after deposition of HDP-SiO2, and the spectrum analysis of re-sputtering induced bridge

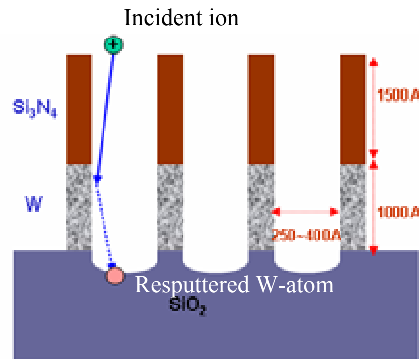

Figure 2: Structure of bit-lines with 37nm (pitch=74nm) and tungsten re-sputtering mechanism in plasma conditions when deposition of HDP-SiO_2

than those of other cells in the array, have been found. We believe that tungsten micro-bridges between tungsten bit-lines (Fig. 1) cause the shift of cell V_{th}. In 37nm technology, the high density plasma has been used to pattern tungsten bit-line and to deposit HDP (High Density Plasma)-SiO_2 as ILD (Inter-Layer Dielectric). Incident ions from the plasma can sputter the tungsten of bit-line and the sputtered tungsten can be re-deposited on the top of etched dielectric layer between bit-lines as shown in Fig2. In order to figure out which process step is dominant in the formation of tungsten micro-bridge, the flux of sputtered tungsten is investigate for several factors such as W thickness, sidewall slope and height of bit-line, and bias power and pressure of equipment, etc. Simulations are performed using in-house tool, PIE simulator [3]. The global model is used in the plasma simulation and Rilley model is used to calculate the ion energy and the angle distribution. The 2D profile simulation using level set method is performed to calculate the tungsten particle distribution by ionic sputtering.

2 Modeling

Fig. 3 shows the overall simulation procedure to analyze the re-sputtering of tungsten from the bit-lines. After obtaining the flux of ion species, IEAD (Ion Energy Angle Distribution) and sputtering yield function is obtained by the plasma simulation and

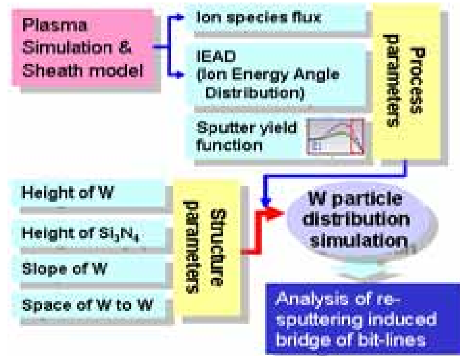

Figure 3: the sequence of simulation to analyze the bridge mechanism using in-house tool, PIE simulator

sheath model, the tungsten particle distribution are simulated for different structure parameters. The angular distribution of incident ion and sputtering yield function are obtained for each plasma conditions.

3 Results and Discussion

Fig. 4 shows the two different angles (α, β) of incident ion. The angular probability of incident ions is maximized at $\beta=90^o$ as shown in Fig.5. But, sputtering yield has maximum value at $\alpha=55^o$ and then decreases with angle α (Fig.6). Fig.7 represents the process conditions for bit line etching and HDP-SiO_2 deposition, and the structural dimensions of bit-line. The flux of re-sputtered tungsten increases as the space

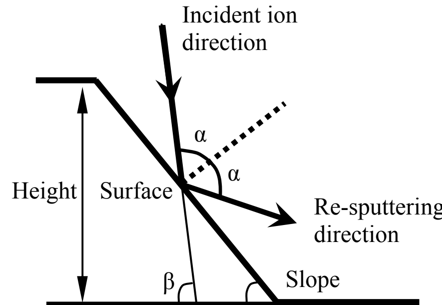

Figure 4: Incident ions sputter the surface of tungsten and re-deposit on the bottom between bit-lines

between bit-lines becomes narrower (Fig.8). The amount of re-deposition at the edge of space is more than that of the center. Fig.9 shows how the flux of re-sputtered tungsten changes by change of source power, bias power, gases and pressure during the bit line formation process proceeds. The flux increases as the source power and pressure increase. Similar results are also obtained in HDP-SiO_2 deposition (Fig. 10). However, the amount of re-sputtered tungsten flux in HDP-SiO_2 deposition is more than 10 times that of etching process. The dependences on the structural parameters

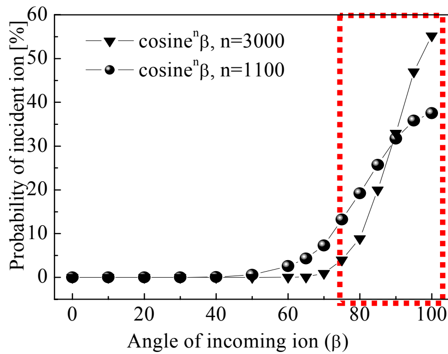

Figure 5: Probability of incident ions for angle of incident ion (β) according to directionality

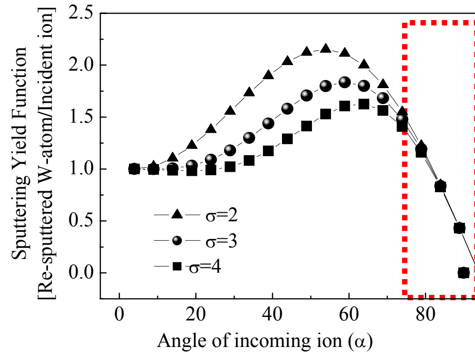

Figure 6: Sputtering yield function for angle of incident ion (α) for sigma values

HDP SiO_2	5000Ws/1800Wb/*AR/*SiH_4/5mT			
Etch	500W/150V/*CL_2/*N_2/*AR/4mT			
Size of W	Height of W	Height of Si_3N_4	Slope of W	Space of W to W
370Å	1000Å	1500Å	85.6°	400Å

Figure 7: Process conditions of etching and HDP-SiO_2 equipment, and dimension of bit-line

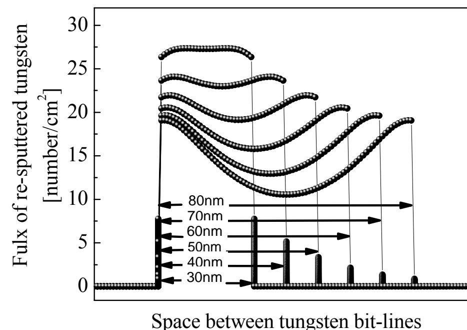

Figure 8: Flux of re-sputtered tungsten for space size.

are shown in Fig. 11. In order to prevent the re-sputtering of tungsten from the bit-lines during HDP-SiO_2 deposition, the buffer SiO_2 is deposited before HDP-SiO_2 deposition. As a result, the bridge-free bit-lines are obtained, and the random bits showing higher V_{th} disappear.

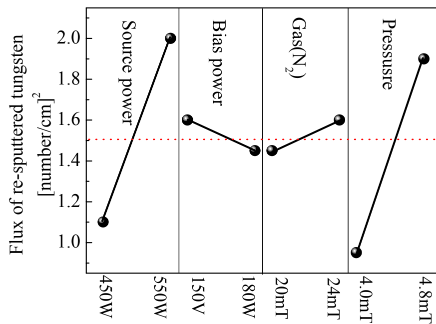

Figure 9: Flux of re-sputtered tungsten as the parameters of etching equipment are increased by 20%

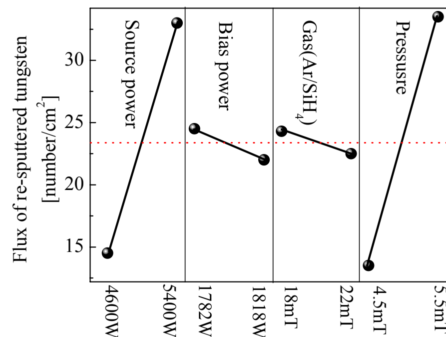

Figure 10: Flux of re-sputtered tungsten as the parameters of HDP-SiO_2 equipment are increased by 20%

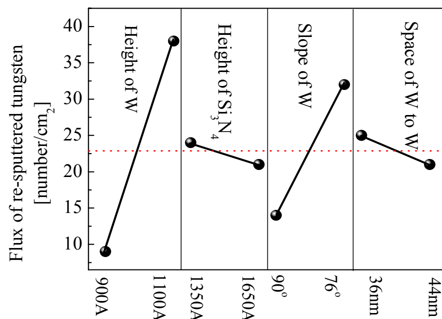

Figure 11: Flux of re-sputtered tungsten as the parameters of bit-line dimension are increased by 20%

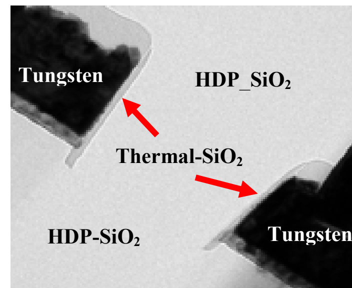

Figure 12: TEM image of bridge-free bit-lines by using thermal-SiO_2 as a buffer layer before deposition of HDP-SiO_2

4 Conclusion

The tungsten re-sputtering from the bit lines under the high density plasma is investigated using in-house tool, PIE simulator, for a high density flash memory with 74nm pitch. Re-sputtering is found to occur during HDP-SiO_2 deposition. By introducing a new buffer oxide before HDP-SiO_2 deposition, bridge-free bit-lines are obtained (Fig. 12).

References

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