High Performance, Strained-Ge, Heterostructure p-MOSFETs

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Abstract

The optimal device structures and channel orientation for nanoscale strained-Ge heterostructure p-MOSFETs, are discussed through detailed Band-to-band-tunneling (including band structure and quantum effects), Low-field Mobility (k.p and Boltzmann Transport), Full-Band Monte-Carlo, and 1-D Poisson -Schrödinger Simulations. The tradeoffs between drive current (ION), intrinsic delay (τ), band-to-band-tunneling (BTBT) leakage and short channel effects (SCE) have been systematically compared in high mobility strained-Ge Heterostructure FETs (H-FETs).

1 Introduction

High mobility channel materials like strained-Si, Ge and strained SixGe1-x are very promising as future channel materials [1]-[6]. Currently, strained-Si is the dominant technology for high performance p-MOSFETs and increasing the strain provides a viable solution to scaling. However, looking into future nanoscale p-MOSFETs, it becomes important to look at novel channel materials, like Ge or strained-Ge, and novel device structures which may perform better than even very highly strained-Si. Most high mobility materials, like s-Ge have a significantly smaller bandgap compared to Si and suffer from higher BTBT leakage, which may ultimately limit their scalability. Strained-Ge heterostructure p-MOSFETs offer a very promising solution to reduce the off-state leakage currents, while maintaining very high carrier mobilities [1]-[2]. In this work, through detailed simulations, we systematically compare different Double-Gate (DG) H-FETs, and identify the optimal device structures, and channel orientations. The devices are also benchmarked to r-Si, s-Si and r-Ge devices.

2 Device Structures And Channel Materials

A common terminology used in this paper is a channel material (x,y) where, x denotes the Ge content in the channel material and y denotes the Ge content in an imaginary relaxed (r) substrate to which the channel is strained (s). E.g. (0.3,0) is a s-SiGe (with 30% Ge content) channel strained to an underlying Si substrate. (0,0.6) is a s-Si channel strained to a r-SiGe (60% Ge content) substrate. In this work, the s-Si was varied from (0,0) r-Si to (0,1) s-Si (100%) and the s-SiGe was varied from (1,1) r-Ge to (1,0) s-Ge (100%).
Fig. 1(a)-(c) show the schematic of the device structures and materials that are investigated. 1(c) is a heterostructure p-MOSFET with a strained-SiGe channel that is sandwiched between two thin Si caps. The bandstructure for a (1,0) s-Ge heterostructure is shown in Fig. 2. The bandgaps (E_G), ladders and effective masses used in this work are taken from [7]-[8].

3 BTBT Leakage

Fig. 3 shows a typical Id-Vg characteristic of a p-MOSFET. The minimum achievable standby leakage ($I_{OFF,MIN}$) is at the intersection of the BTBT leakage with the subthreshold leakage. To accurately estimate $I_{OFF,MIN}$ for different materials and structures, we performed detailed BTBT simulations, which take into account bandstructure information, quantum mechanical (QM) effects and the direct-indirect valley transitions. Typically, $I_{OFF,MIN}$ increases monotonically with increasing strain due to the rapid reduction in the EG. In Fig. 4, (1,1) r-Ge shows higher leakage than (1,0) s-Ge due to the low lying Γ-valley, which allows for a large direct BTBT leakage component. (0,1) s-Si has the highest $I_{OFF,MIN}$ because of an extremely small E_G. Fig. 4 shows that we can further reduce the leakage component in (1,0) s-Ge MOSFETs by using a heterostructure DG MOSFET. For a Ge thickness (T_{Ge}) <~2nm, the $I_{OFF,MIN}$ rapidly drops by over an order of magnitude due to the large quantization, which increases the effective E_G (Fig.5). Thus, by varying the Si capping layer thickness ($T_{Si,Cap}$) and the Ge thickness (T_{Ge}) we can effectively use the heterostructure double-gate geometry to control the device leakage.

4 Short Channel Effects (SCE)

Due to its higher dielectric constant (κ_S), Ge shows worse SCE compared to Si. The main concern with heterostructure FETs is the reduced electrostatic control due to the channel being further away from the gate insulator interface. As shown in the Fig. 6, for a given T_S and L_G, several sets of simulations were performed, where T_{Ge}/T_S goes from 0% (surface channel Si) to 100% (surface channel Ge). Then, using T_S and L_G as parameters, the Drain Induced Barrier Lowering (DIBL) and Su-threshold Slope (SS) are plotted in Fig. 7 (a)-(b). Compared to the Si control, the surface channel Ge ($T_{Ge}/T_{Si,cap}$= 100%) shows slightly worse SCE due to its higher κ_S and the worst SCE occurs in the device where T_{Ge}/T_S = 25%, where the channel is the farthest from the gate. The SCE is around ~5-10% worse for the worst-case (25%) device, meaning that its L_G would have to be ~5-10% longer or TS ~5-10% thinner to achieve the same electrostatic control compared to the surface channel. However, the overall SCE values for all the DG FETs are excellent and quite comparable.

5 Low Field Mobility

The low-field mobility was calculated from a self consistent solution of the 1-D Poisson-Schrödinger (k.p) equation and Boltzmann-Transport within the 2-D Brillouin Zone of each sub-band. Four important scattering mechanisms are considered: acoustic phonon, optical phonon, surface roughness and alloy scattering [9]. Fig. 8 shows the mobility as a function of inversion carrier density for different H-FETs with TS=5nm. The simulation reveals an optimal s-Ge thickness. Due to the reduced surface roughness scattering, the H-FET with ~1.5nm Si cap and ~2nm s-Ge layer has the highest low-field mobility among all the DG p-MOSFETs.

6 Full-Band Monte-Carlo (Drive Currents/Intrinsic Delay)

In order to accurately estimate the transport in highly scaled MOSFETs, Full-Band Monte-Carlo simulations need to be performed [10]. As shown in Fig. 9, for the (001) surface considered in this work, the I_{ON} for the channel along the [100] direction is significantly higher than the [110] direction. The I_{ON}, for the different s-SiGe H-FETs are shown in Fig. 10. Due to the lower capacitance and worse SCE, the heterostructures shows a slightly lower drive compared to the surface channel MOSFET. Ultimately, device switching speed is estimated by the intrinsic gate delay (CV/I). As seen in Fig. 11, due to its lower capacitance and high drive

current, the optimal delay is obtained in a s-Ge H-FET with TGe ~2nm. A plot of the switching frequency vs. the minimum standby leakage achievable is a good benchmark to compare different device structures and channel materials. In Fig. 12, we find the performance of (0,0.6) s-Si and (0.6,0) s-SiGe p-MOSFETs are very comparable. However, as we scale to higher mobility materials, s-SiGe rapidly outperforms s-Si. Further, by using a s-Ge heterostructure p-MOSFET, the switching frequency can be increased (>2X) and the standby leakage can be further effectively reduced.

7 Conclusions

The optimal DG s-Ge heterostructures for future nanoscale DG p-MOSFETs are obtained through detailed BTBT (including band structure and quantum effects), Low-field Mobility, Full-Band Monte-Carlo and 1-D Poisson-Schrodinger Simulations. The tradeoffs between drive current (I_{ON}), intrinsic delay (τ), band-to-band tunneling (BTBT) leakage and short channel effects (SCE) have been systematically compared. Our results show that the best channel material and device structure for optimal performance can be obtained in a sub-20nm, (1,0) s-Ge heterostructure p-MOS DGFET with an ultra-thin ~2nm strained-Ge channel.

8 Acknowledgements

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9 References

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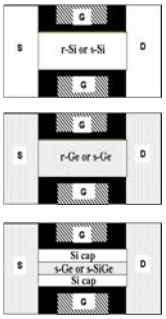


Fig1 (a), (b) and (c): Device structures – surface channel and heterostructures with different channel materials

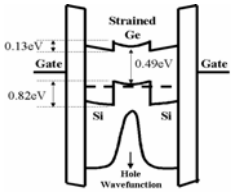


Fig2: Band structure for the r-Si/s-Ge/r-Si heterostructure

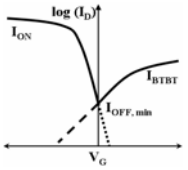


Fig3: $I_{(OFF,\ min)}$ is the minimum achievable leakage in a MOSFET

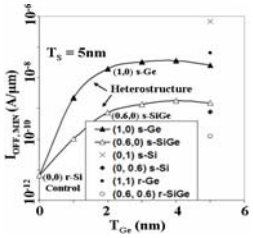


Fig4: $I_{(OFF,min)}$ for the different materials compared to the heterostructure

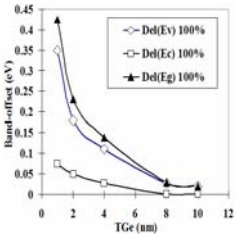


Fig5: 'Effective bandgap' increases due to quantization

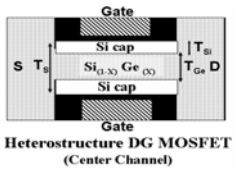
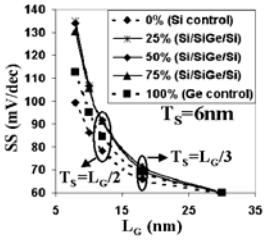


Fig6: To benchmark the SCE, the ratio of TGe/Ts was varied from 0% (surface channel Si) to 100% (surface channel Ge).



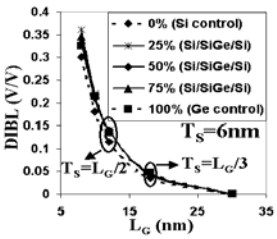


Fig7 (a) and (b): Subthreshold Slope and DIBL as a function of channel length

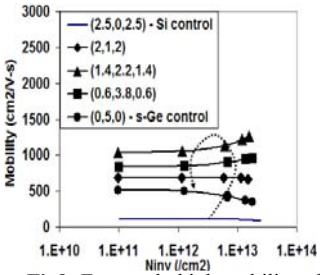


Fig8: Extremely high mobility of the 2nm s-Ge heterostructure FET

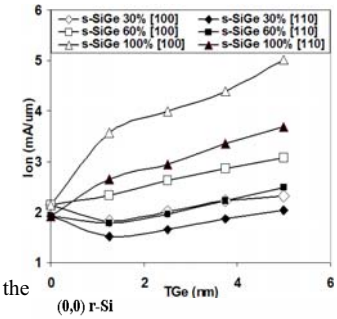


Fig9: $I_{(ON)}$ for s-SiGe hetero-FETs. [100] is the preferred channel orientation on (001) surface.

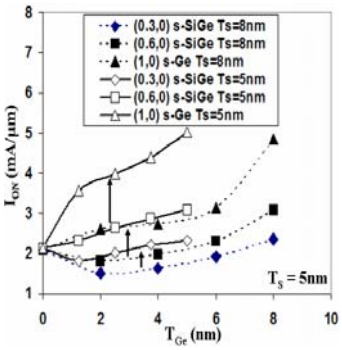


Fig10: Effect of Ts variation on the $I_{(ON)}$ of the heterostructure.

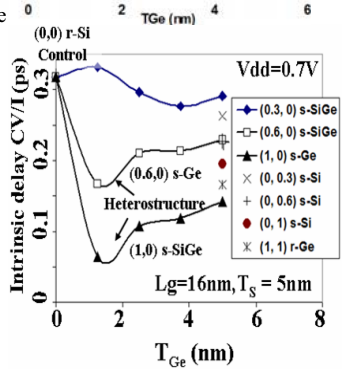


Fig11: Intrinsic delay of different materials. ~2nm H-FET is optimal.

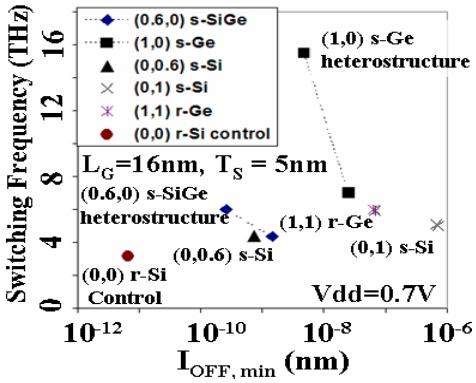


Fig12: Switching frequency vs leakage current to benchmark the different materials and device structures.