Nanomanufacturing Technology and Opportunities Through Physically-Based Simulation

Mark R. Pinto
Applied Materials, USA
mark_pinto@amat.com

1 Introduction

The semiconductor industry has clearly moved into the era of nanoelectronics where the "the understanding and control of materials at the sub-100nm level" – the best established definition of nanotechnology [1] – is essential to maintaining Moore's Law. However nanoelectronics, like many other applications for nanotechnology, requires more than making single devices in small areas. To be commercially relevant, structures must be manufactured in volume and/or over large areas. And perhaps most fundamentally they must be produced at ever lower costs to drive adoption of new applications, grow end markets and provide the source of investment in next generation technology. In many instances, the invention of an appropriate manufacturing method may be of equal importance to the underlying device concept – there is perhaps no better example of than that of the IC itself where both Kilby (first realization) and Noyce (manufacturable process) are recognized as its primary inventors. We will define these methods of realization as "nanomanufacturing technologies" – i.e. the materials, process and measurement tools and technologies that deliver the required scale, cost, reproducibility and reliability to manufacture successful nanotechnology-based products.

Physically based simulation (including TCAD) has undeniably played a critical role in the progress of semiconductor ICs. With the increased complexity of the challenges ahead, together with ever increasing development costs, there is an opportunity for an even greater role. The same is true for other applications of nanotechnology where simulation may help discover solutions that enable new markets – there is perhaps no better advertisement for simulation that the definition of nanotechnology above. However to have the fullest impact, just like the difference between making one device and billions, simulation needs to move beyond just adding physics to reproduce I-V characteristics at the next CMOS node. Below the nature of these challenges and some possible roles for simulation in advancing nanomanufacturing technologies are discussed.

2 Nanoelectronics

The IC industry has continued pushing component count per die and scaling constantly for over 40 years since Moore published his seminal projection in 1965. For the industry to have invested so heavily, there has to have been major commercial benefits to scaling – these include product form factor, performance, power per computation, reliability – but none has been as important as the reduction in cost per transistor or bit,

the foundation of Moore's prediction. Especially now in the era when consumer applications (cell phones, MP3, digital TV, etc.) and penetration into emerging economies are primary factors behind industry growth, continued reduction in cost/transistor is the overwhelmingly critical factor in sustaining the scaling roadmap.

As with other applications that lend themselves to nanomanufacturing discussed below, it is instructive to examine the components of unit production cost, i.e.

$$\text{Cost / Function} = (\text{Cost / Area}) / (\text{Function / Area}) \quad (1)$$

In the case of nanoelectronics, the functional unit of interest is a transistor or bit. Figure 1 shows the number of transistors produced yearly as well as the average cost per transistor from 1968-2002 [2]. This reduction has followed a traditional learning curve where increasing scale and units accompanies the decreasing cost – for the IC, the cost per transistor has reduced by ~28% for every doubling of volume. Recent estimates for the price per memory bit are on the order of 1 billionth of a dollar, i.e. 1 nano-dollar.

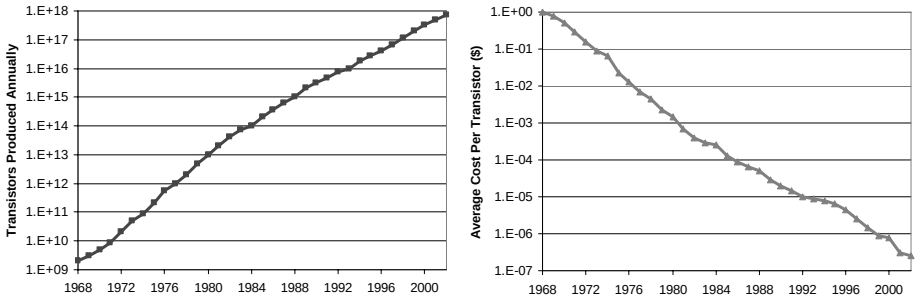


Figure 1 – Historical transistor (a) total annual production and (b) average cost [2].

The primary driver of cost per transistor (or bit) reduction is dimensional scaling or the denominator in equation (1). Much of the research on TCAD has also focused on maximizing transistor density through design of processes that scale to smaller dimensions and of devices that meet corresponding integration requirements. However as the roadmap is pushed further, new considerations arise where simulation can also have broader impact – most importantly sub 100nm patterning, new materials and variability.

Optical patterning is finally nearing limits with exposure wavelength limited to 193nm, and production-worthy replacements not yet in sight. Since 90nm, the focus has thus been on utilizing higher NA lenses and the process k1. As limits are approached, it is essential to consider more complex integration to push densities including steps such as planarization and extra patterning films before exposure and etch afterward. These sequences become even more complicated when using various forms of double patterning [3] where multiple deposition and etch steps are included for every design

layer. Integrated, physically based simulations – taking advantage of every point of leverage in each step and each tool – hold the promise of helping push to ultimate printability limits.

Beginning with the 130nm CMOS node and Cu-based interconnect, the industry has begun a more rapid introduction of new materials to circumvent straight forward scaling limitations such as transistor on-off, gate leakage, RC parasitics and electromigration. Perhaps most prominent are the new materials being explored for scaled transistors – e.g. high-k/metal gates and strain engineering – where it is impractical to fully explore all possible structures and materials and enormously expensive even to evaluate subsets of promising candidates. Here various levels of simulation can play a critical role – from first principles simulations to understand band structures, quantization and scattering to full 3D transport to optimize the coupled geometrical effects from stress inducing overlayers, isolation, epi source/drains and substrates. Figure 2 shows a recent result where selective SiGe PMOS was combined with a compressive silicon nitride overlayer and optimized using simulation to achieve an 85% increase in drive current at a fixed off current [4]. While initially used for high speed applications like server microprocessors, the option of trading off leakage for performance (e.g. in figure 2b one can achieve 100x improvement in Ioff at a fixed Ion) have promoted the use of strain more universally.

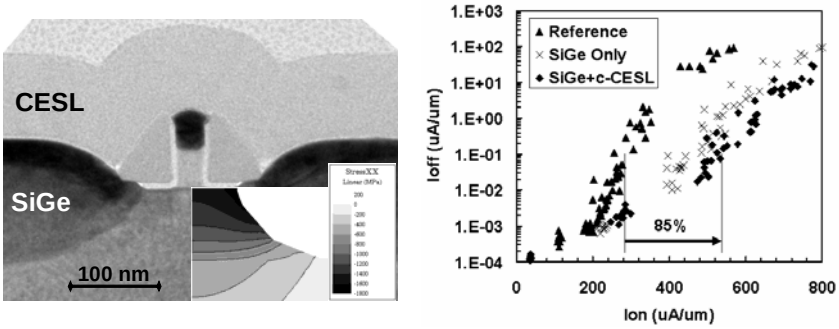


Figure 2 – Strain engineering. (a) TEM of PMOS with SiGe in S/D and c-CESL showing simulated stress contours used to determine local mobilities (b) experimental on-current vs. off-current using different strain enhancement techniques [4].

It is important to note that the denominator in equation (1) also intrinsically includes the effect of device yield – specifically the appropriate measure is functional units per area. In the past some fairly simple methodologies were used to capture the effect of device variability throughout the design chain, and hence its effect was not really a major consideration in technology development. However again beginning at 130nm and getting progressively worse into sub 100nm nodes, variability has become a first order issue with implications for tool, process, device and circuit design as well as

metrology, inspection and electrical test. Simple geometric rules and corner cases have become inadequate to provide an effective foundation for design.

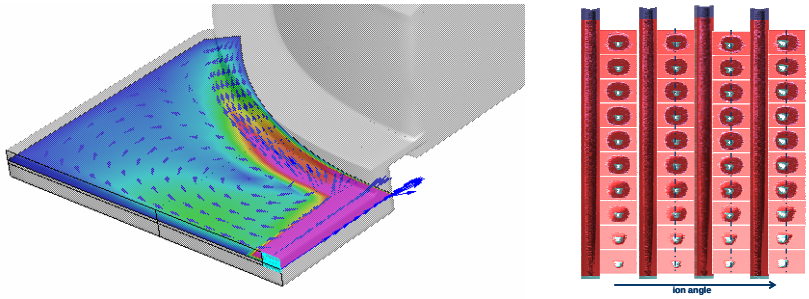
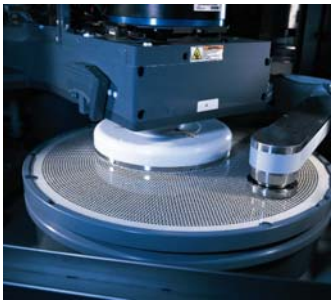


Figure 3 – Examples of equipment simulations where process uniformity is a primary concern (a) flow contours in a 3D epitaxial simulation showing the effect of source gas design [5] and (b) deep trench plasma etch simulations showing the effect of off angle ions on trench shapes towards the edge of a 300mm wafer [6].

While not as dramatic an effect as scaling, process cost – the numerator in equation (1) – has also played a significant role in bringing down the cost of a transistor. In fact because many of the innovations required to sustain scaling come at increased process complexity, the cost of unit process steps must be continuously reduced just to remain near even on total process cost. Several key factors can positively affect process cost per area – e.g. substrate size, tool+process throughput, consumable costs – and all of these are preeminent issues for equipment design. Furthermore they are intrinsically coupled back to the denominator in (1) and most importantly to variability. It should not be surprising for instance that it is harder to design equipment that keeps uniform plasmas over larger wafers or that higher deposition throughput can come at the cost of increased thickness variation.

Equipment modeling can play a critical role in gaining fundamental insight and better tool design by addressing the combined challenges of both the numerator and denominator in (1). Figures 3 and 4 show some typical examples of where equipment simulation was used in recent technologies – deep trench etch, epitaxial deposition and chemical-mechanical polishing (CMP). In each case variability control was the most difficult design target parameter and the models required to gain understanding involved at least both field (electrical, mechanical and/or thermal) and chemistry simulation, as well as flow in the case of etch and epitaxy. The epitaxy simulations for instance typically take up to 100 hours on a 4 processor compute system for a single condition.



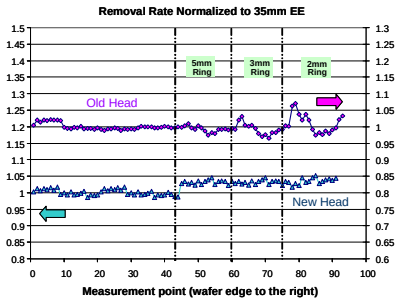


Figure 4 – Chemical mechanical polishing (CMP): (a) Applied Reflexion® LK CMP system and (b) finite element based simulations of CMP material removal rates for two different multizone head designs demonstrating better center to edge uniformity with new design out past the 2mm edge ring for a 300mm wafer [7].

Finally a more critical equipment/process design consideration has become environmental sustainability. While semiconductors have had an overall positive effect on the economy and environment – e.g. through increased productivity, global networked communications that avoid travel, sophisticated system controls, solid state memories and others – it is still incumbent on the industry to minimize the overall impact of IC processes. Although adding an additional design challenge, minimizing energy, consumables and by-products almost always results in reduced cost per wafer. Addition areas of focus for improved sustainability include development of processes with lower environmental impact as well as abatement and material reclamation systems. Equipment simulation is being increasing leveraged in all these areas.

3 Nanomanufacturing Technology Beyond ICs

Another example of the impact of nanomanufacturing technology and one inspired by ICs is the LCD flat panel display (FPD). It is almost hard to remember now that even 10-15 years ago flat panel computer monitors were outrageously expensive and flat panel home TVs were just a dream. However a revolution has taken place in production cost which has brought larger and larger FPDs into the realm of consumer affordability. This reduction has been driven almost exclusively through cost per area along with evolutionary improvements in film quality and control – specifically by increasing substrate size while maintaining equipment productivity. In fact for most nanomanufacturing applications other than nanoelectronics, cost per area is a dominant or more equal driver for total cost per function reduction as compared to the function per area denominator that dominates IC information processing.

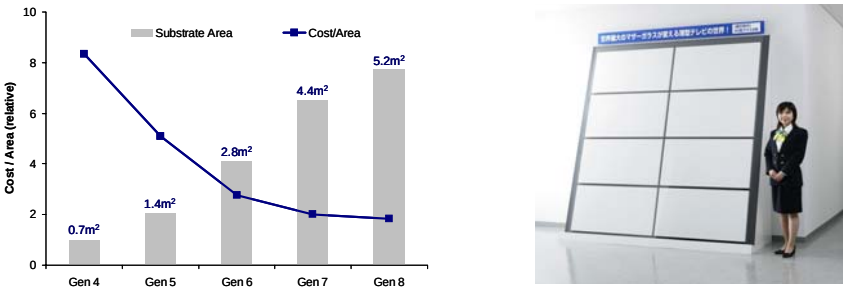


Figure 5 – LCD flat panel production (a) PECVD cost/area reduction with glass size (b) Gen 8 glass substrate used at Sharp Kameyama fab (courtesy Sharp Corporation).

Figure 5a shows a deposition process cost/area reduction of > 4x as glass substrates have been scaled upwards from < $1m^2$ (Gen 2) to > $5m^2$ (Gen 8) or a 25% per year growth in size for 14 years. Also shown is a picture of one of the largest LCD TFT flat panel substrate currently in production at the Sharp Gen 8 fab in Kameyama, Japan which can produce six 52" TV panels on one sheet of mother glass. In order to achieve the cost reductions, the deposition tools not only have to work over larger area but they also need at least maintain ~50nm uniformity as well as throughputs in excess of 50 substrates/hour – or the equivalent glass to cover a full size international football pitch per day.

Perhaps obvious but nonetheless surprising when first visualized, the equipment needed to produce substrates like that in figure 5b needs to be proportionally scaled upwards from the IC industry equivalents. Figure 6 shows PECVD and PVD systems for Gen 8 LCD production. Clearly equipment design – especially with respect to variability – for these systems is an enormous challenge. In fact the design problem is further complicated by the comparative scale of RF wavelengths and the dimensions of these chambers. Specifically to avoid surface standing waves and their nearly unmanageable effect on non-uniformity, the RF frequency must exceed the criterion as follows:

$$\lambda_0 (f_{RF}) >> \lambda_c \text{ (Chamber dimensions)} \qquad (2)$$

where for Gen 8 FPD substrates (2160 x $2140mm^2$), λ_c ~ 11m. This implies that to avoid surface standing waves, RF frequencies must be selected < 20MHz which introduces additional equipment design and process constraints, e.g. throughput.

In addition to the design of the chamber itself, another challenge is material utilization which is a significant cost of manufacturing, much more than for ICs. Whether it is the gases used for layer formation and for chamber cleaning or the sputter targets, there is an enormous benefit to designs that minimize material consumption. Taking sputtering as an example, it was not uncommon to get < 30% material utilization at Gen 6 before

having to replace the target. Through innovative designs based on physically based analyses, this waste is being significantly reduced for Gen 8 and above.

Figure 6 – Large area nanomanufacturing deposition equipment for LCD flat panel displays (a) PECVD cluster tool for the TFT array (b) in-line PVD TCO for color filters.

The rising cost of energy together with the aforementioned widespread interest in environmental sustainability has brought renewable energy solutions back to the forefront of the R&D and business agenda. Examples of renewable energy product categories that can benefit from nanomanufacturing are photovoltaics (PV) for electricity generation and solid state LEDs to minimize energy dissipation for lighting. In both these cases, the critical factor to growing adoption is driving down costs – for PV it is cost per Watt whereas for solid state LEDs it is cost per Lumen.

Focusing on PV, we can decompose manufacturing cost per Watt into a numerator and denominator after (1),

$$\text{PV Cost / Watt} = (\text{Cost / Area}) / (\text{Watts / Area}). \quad (3)$$

Like displays, PV cost per area can be driven by large area nanomanufacturing equipment like that shown in figure 6a, adopted to thin film absorber layers on thicker glass (or alternatively to trays of wafers). Watts per area corresponds directly to conversion efficiency which can be driven by improvements to materials, device structures and even better manufacturing uniformity. Figure 7a shows an example of material innovation where a tandem a-Si/uc-Si junction is used to capture more of the photon spectrum than just a single a-Si thin film cell, thereby improving module conversion efficiencies. Using tools like that in figure 6a, complex thin film tandem cells can thereby be realized on large solar modules like in figure 7b at production costs quickly approaching $1/Watt.

Several important observations can be made about (3) that suggest promising opportunities for applying physically based simulation more broadly to the PV field. First – and again like ICs – improvement in efficiency (the denominator) can come at a steep price in terms of process cost (the numerator) – either in number of steps or in lower throughput of tools to achieve higher quality deposited materials. Second it is fair to state that the PV field has virtually been ignored by the simulation communities (and

especially when coupled to low cost processes). One may therefore expect there to be enormous potential leverage to be gained from simulation for PV, for instance in understanding the role of material or interface parameters, in predicting reliability, and in optimizing process cost versus efficiency. Note also that unlike ICs, the denominator in (3) has some bounded theoretical limits (certainly < 1) while the numerator, in principle, has unlimited potential for improvement. Therefore it should be expected that PV equipment simulation and productivity improvements should have a significant influence long into the future.

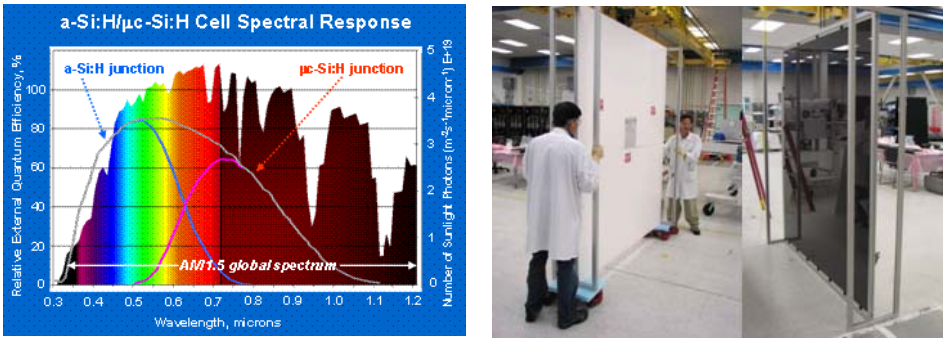


Figure 7 – Thin film silicon solar cells (a) spectral response of a-Si/uc-Si tandem junction (b) Gen 7 panel produced by a large area PECVD tool like that in figure 6a. Note the color of the panel is dark gray indicating the absorber is not pure a-Si.

4 Summary and Conclusions

The wide spread adoption of products like sub 100nm CMOS ICs, flat panel displays and photovoltaics, depend on reproducible and cost effective nanomanufacturing technologies. The challenge of driving cost per function down past critical price points requires understanding and coupled optimization of basic materials, equipment and processes at scales well below 100nm (and variability control to even finer scale), suggesting an ever increasing potential from physically based simulation. However as with the differences in the respective equipment solutions, it is important to reframe the scope of simulation to have the maximum impact on new application areas.

References

[1] http://www.nano.gov/html/facts/whatIsNano.html.
[2] G. Moore, ISSCC 2003 (see http://www.intel.com/technology/mooreslaw/index.htm).
[3] W. Arnold et. al., Proc. SPIE, vol. 6518, 2007.
[4] L. Washington et. al., IEEE Electron Device Letters, June 2006.
[5] J. Grayson, Applied Materials (unpublished).
[6] P. Stout and U. Mitra, Applied Materials (unpublished).
[7] K. Hughes et. al., Applied Materials ET Conference Abstract, May 2007.