Novel Asymmetric Raised Source/Drain Extension MOSFET

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***Abstract*— A novel asymmetric MOSFET structure is proposed which provides an excellent tradeoff between current drivability and manufacturability for planar MOSFET technology. To achieve this, the "corner effect" is utilized to suppress short channel effects, while degradation in current drivability caused by the corner effect is avoided by an asymmetric design. Using simulation, it is shown that this structure enlarges the tolerance for the junction depth of source/drain extensions by a factor of three, without sacrificing current drivability, compared to the optimal symmetric structure also found in this work. This asymmetric structure is a superior design strategy for planar MOSFETs and can be considered as one of the most promising candidates for 32nm-node MOSFETs.**

I. Introduction

Shrinkage of conventional planar MOSFETs has required increasingly shallow source/drain extension junctions to suppress short channel effects (SCE). However, junction depth reduction increases extension resistance, which can limit current drivability.

To realize extremely shallow junctions and low resistance simultaneously, we have already proposed a novel symmetrical raised source/drain extension structure for 32nm-node MOSFETs[1]. This structure is a superior design strategy for planar MOSFETs because it achieves virtually zero junction depth without increasing extension resistance.

However, despite its low resistance, current drivability is low in the case of zero junction depth because of the "corner effect" which generates a potential barrier at the gate corners (cf. Fig. 1) due to their curvature[2], and which occurs in grooved-gate MOSFETs [2], [3], [4]. Therefore, SCE and current drivability remain a tradeoff requiring determination of an optimum junction depth. The depth and its design concept, however, have until now not been provided.

In this paper, we derive an optimal junction design for the above symmetrical MOSFET, and show that an accuracy of about $\pm$1nm is needed for the junction depth. Building on this, an asymmetric structure is then proposed to enlarge the tolerance without sacrificing current drivability. This structure can be regarded as a superior design strategy for planar MOSFETs.

II. Optimal Symmetric Structure

The simulation structure for the symmetrical MOSFET is defined as shown in Fig. 1. Compared to the conventional raised source/drain extension MOSFETs [5], [6], this structure features: (1) elevated source/drain extensions with facets separated from the gate stack with low-k materials, (2) gate electrodes having overlaps with facet bottoms, and (3) minimum junction depth in the extensions. The facets and the low-k materials reduce the parasitic gate capacitance; the overlaps between the gate electrode and the facets lower the parasitic source/drain resistance by means of the accumulation layer formed in these overlap regions which connects the inversion layer with the highly conductive regions in the extensions.

The design parameters of this structure are also shown in Fig. 1. Optimization was performed for these parameters, especially for N_{SUB}, N_{EX}, and X_J. For simplicity, uniform doping profiles were applied to respective regions in the structure. The evaluated ranges of the respective parameters, and the other structural constants are summarized in Table I.

Maximum drain current I_{on} was sought in this optimization under the conditions: subthreshold slope (S)$<$ 0.1V/decade, drain-induced barrier lowering (DIBL)$<$ 0.1V, and $\Delta V_T <$ 0.1V where ΔV_T is the shift in threshold voltage caused by a 4nm (20% of the total) gate length reduction. The target gate length is 20nm; the gate material is assumed to be metal; and, by choosing the material, it is also assumed that we can choose a gate work function ϕ_m. Due to this assumption, the threshold

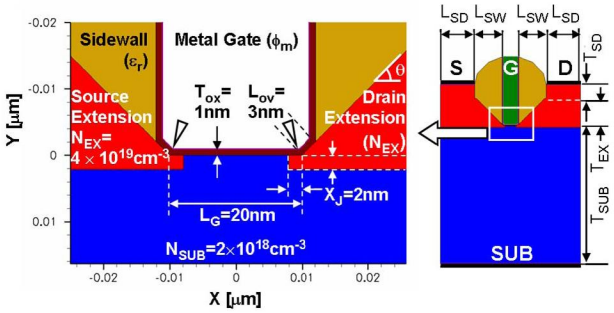

Fig. 1. Simulation structure of the symmetrical MOSFET with design parameters. The gate corners are indicated by the open triangles. X_J is the junction depth of the extensions, N_{EX} the doping concentration in the extensions, N_{SUB} the substrate doping concentration. The physical gate insulator thickness T_{ox} was assumed to be 1nm, and the gate work function ϕ_m to be adjustable within 4.05 to 5.2eV to obtain a desired V_T. Other values in this figure are the results of optimization. The right inset is the overall structure.

TABLE I

DESIGN PARAMETERS AND THEIR EVALUATED RANGES

	Parameter	Evaluation Range
Gate electrode	Work function (ϕ_m)	4.05eV
	Gate length (L_G)	20nm
	Gate overlap length (L_{ov})	0··10nm
Gate insulator	Physical thickness (T_{ox})	1nm
	Dielectric constant (ϵ_{ox})	3.9
Substrate	Impurity concentration (N_{SUB})	$\{0.2\cdot\cdot5\}\times10^{18}$cm^{-3}
	Thickness (T_{SUB})	0.2μm
Source/drain extensions	Impurity concentration (N_{EX})	$\{1\cdot\cdot10\}\times10^{19}$cm^{-3}
	Junction depth (X_J)	-10··5nm
	Thickness(T_{EX})	40nm
	Facet angle (θ)	25° · ·55°
Source/drain	Impurity concentration (N_{SD})	$= N_{EX}$
	Thickness (T_{SD})	20nm
	Electrode length (L_{SD})	50nm
Sidewall	Dielectric constant (ϵ_r)	3.9, 7.5
	Width(L_{SW})	40nm

voltage can be shifted to a positive value by choosing ϕ_m even if the initial design results in negative threshold voltage for an n-channel FET. Therefore, 4.05eV was used for ϕ_m throughout this paper. We denote as V_T a gate voltage that allows a drain current of 40nA/μm, and assume that V_T can be positive by choosing an appropriate ϕ_m. I_{on} is defined at a constant gate overdrive voltage of 0.8V, i.e. $V_{GS} - V_T = V_{DD} = 0.8$V. As transport models, the drift-diffusion (DD) model calibrated for our conventional planar MOSFETs ($L_G = 40$nm) and the hydrodynamic (HD) model were used.

Examination of various combinations of these parameters revealed that the best tradeoff between I_{on} and ΔV_T was given by the junction depth at which the corner effect is at the point of being eliminated. The optimum depth was found to be 2nm for the structure in Fig. 1. In this design, the potential at the source-side corner does not act as a barrier for the carrier injection from the source. Similarly, the drain-side corner does not prevent the drain depletion layer from spreading out to the channel. Therefore, to achieve SCE supppression, X_J must be as small as possible, just as with conventional planar MOSFETs, and N_{EX} should be moderate.

Figure 2 shows the X_J dependence of I_{on}, S, and V_T. The reduction in I_{on} for deeper X_J is due to SCE that cause a negative shift in V_T and, consequently, lower the applied gate voltage given as $V_T + 0.8V$. If we assume the allowable V_T variation is $\pm$0.1V, the tolerance for X_J is about $\pm$1nm.

If we take into account realistic gradients in the impurity concentrations, the optimum X_J may be larger than 2nm, yet its actual tolerance seems close to this estimate. This tolerance is therefore expected to be one of the yield determinant factors in future mass-production.

III. NOVEL ASYMMETRIC STRUCTURE

To enlarge the above tolerance, we propose a novel asymmetric structure as shown in Fig. 3. This structure is characterized by positive $X_{J,S}$ (see Fig. 3 for definition) and negative $X_{J,D}$ to utilize the corner effect only on the drain side. To achieve this concept, the following observations were performed.

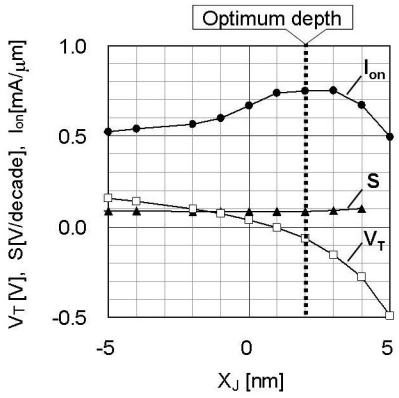

Fig. 2. X_J dependence of I_{on}, S, and V_T: decreases in I_{on} and V_T in positive X_J are due to the V_T roll-off, and those in negative X_J to the corner effect. A 1nm shift in X_J from the optimum depth causes an approximately 0.1V shift in V_T.

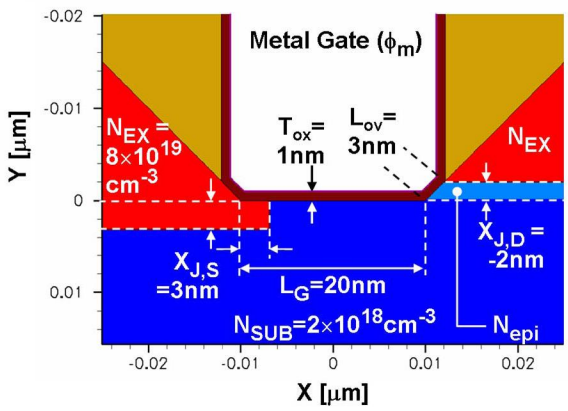

Fig. 3. Simulation structure for the asymmetric MOSFET: $X_{J,S}$ and $X_{J,D}$ are the respective junction depths, N_{epi} was assumed to be 2×10^{16}cm^{-3} for auto-doping during epitaxial growth [1] . Other parameters are in common with those in Fig. 1.

A. *Effects of source-side and drain-side corners*

The effects of corners on the respective sides were examined independently. Figures 4(a) and (b) show the dependence of I_{on} and S on the junction depth of the respective sides. In Fig. 4(a), the current drivability for shallower junctions is shown to be limited mainly by the source-side corner. The increase in S with negative $X_{J,S}$ as shown in Fig. 4(b) indicates the existence of a potential barrier at the source-side corner since the increase in S is due to the locally increased depletion capacitance caused by the curvature of the corner, thus indicating a local increase in V_T [2]. Meanwhile, Fig. 4(b) shows that only the drain-side corner contributes to SCE suppression. Therefore, negative $X_{J,D}$ is found to suppress SCE with a small decrease in I_{on}.

The mechanism of current drivability degradation due to the source-side corner is analyzed as follows. Figures 5(a) and (b) show respectively the distributions of the electrostatic potential and the electron concentration along the drain current path from the source to the drain. Two cases are compared here:

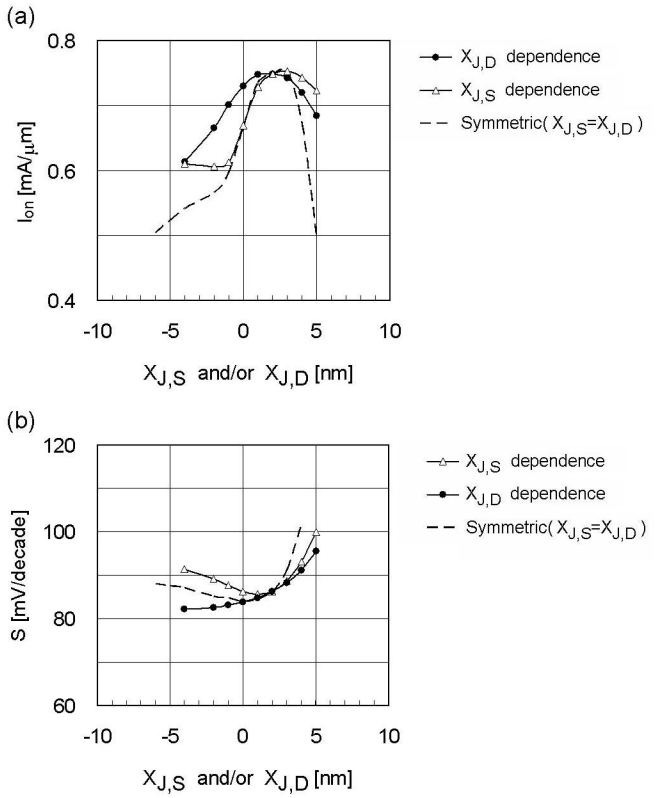

Fig. 4. Dependence of (a) I_{on} and (b) S on $X_{J,D}$ and $X_{J,S}$ computed for the structure in Fig. 3: $X_{J,S} = 2$nm when $X_{J,D}$ is varied, and $X_{J,D} = 2$nm when $X_{J,S}$ is varied. The broken lines are for the symmetric structure in Fig. 1. $N_{EX} = 4 \times 10^{19}$cm^{-3} for all these curves. The other parameters are shown in Fig. 1, and are common to all these curves.

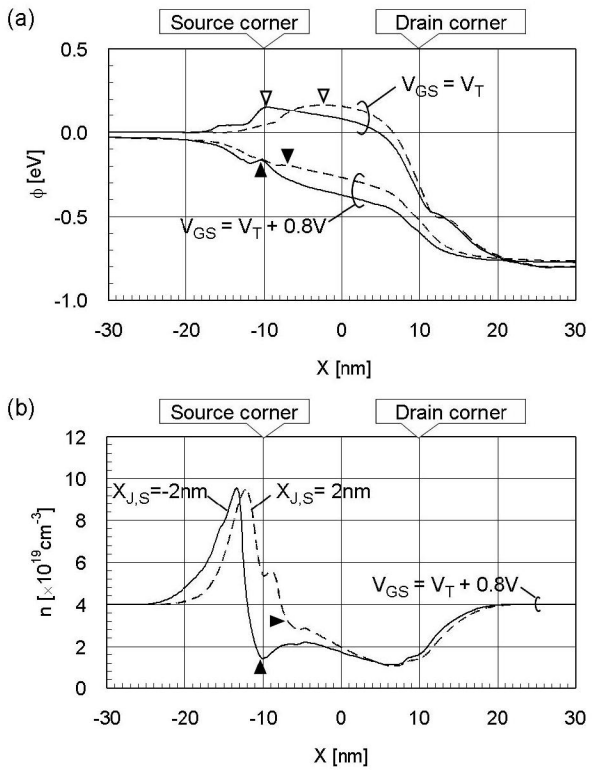

Fig. 5. Distributions along the drain current path of (a) electrostatic potential and (b) electron concentration computed for the structure in Fig. 3 with $X_{J,S} = 2$nm (broken lines) and -2nm (solid lines): $X_{J,D} = 2$nm, $N_{EX} = 4 \times 10^{19}$cm^{-3}, and $V_{DS} = 0.8$V for all the curves. The source and drain terminals of the current paths are located outside of this figure. The open and closed triangles point to the peaks of the potential barriers between the source and the channel at each bias condition.

when $X_{J,S} = 2$nm and -2nm. $X_{J,D}$ is 2nm for both cases.

At $V_{GS} = V_T$, the peaks of the potential energy barriers between the source and the channel (indicated by open triangles) are almost the same height between these two cases as shown in Fig. 5(a), since V_T is defined by the drain current.

At $V_{GS} = V_T + 0.8$V, the peak of the potential barrier for $X_{J,S} = -2$nm locates at the source-side corner, while that for $X_{J,S} = 2$nm is near the metallurgical junction between the extension and the substrate as indicated by the closed triangles. Despite application of the same gate overdrive voltage, the electron concentrations at these barrier peaks are different as shown in Fig. 5(b). This difference is due to the curvature of the corner. Regarding the corner as a part of a cylindrical MOSFET, the sheet carrier concentration n_s of the inversion carriers at the corner is roughly related to the curvature as[2]:

$$n_s = \frac{\epsilon_0 \epsilon_{ox}}{(r + T_{ox}) \cdot ln\left(\frac{r + T_{ox}}{r}\right)} (V_{GS} - V_T) \quad ,$$

where ϵ_0 is the permittivity in vacuum, ϵ_{ox} is the relative dielectric constant of the gate insulator, and r is the radius of curvature of the interface between the gate electrode and the gate insulator. As given by this expression and with $V_{DS} = 0$V, the sheet carrier concentration at the corner is lower than that in the flat channel. A reduced number of inversion carriers are injected into the channel when V_{DS} is increased[7]. Thus, this reduction in carrier concentration is considered to be the principal factor in current drivability degradation.

B. Effects of impurity concentrations in the extension

Figure 6 shows the dependence of I_{on} and V_T on $X_{J,D}$ for two of the N_{EX} values. It should be noted that V_T is almost independent of N_{EX} if $X_{J,D}$ is negative. This is because SCE are suppressed by a potential barrier at the drain-side corner. Therefore, by employing negative $X_{J,D}$, N_{EX} can be higher than the optimum value for the symmetric structure in Fig. 1 without degrading SCE. Meanwhile, I_{on} is increased by increasing N_{EX} as shown in Fig. 6 due to decreased parasitic resistance in the source extension, especially in the vicinity of the gate electrode. From these observations, optimum $X_{J,D}$ is found to be -2nm at which depth its tolerance can be maximized up to ± 3nm for a 0.1V shift in V_T without sacrificing I_{on}.

Suppression of SCE by the drain-side corner allows $X_{J,S}$ to be deeper. Figure 7 shows that $X_{J,S}$ is optimum at 3nm, at which depth its tolerance can be also increased up to ± 3nm.

By using this optimized asymmetric design, V_T roll-off is also reduced as shown in Fig. 8. Gate length tolerance is increased from ± 5nm to ± 6nm for a 0.1V shift in V_T.

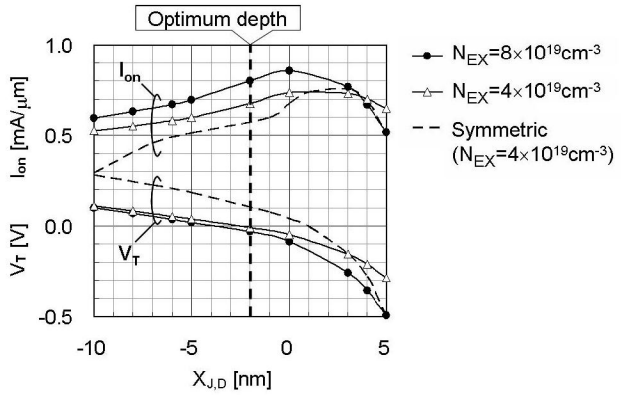

Fig. 6. $X_{J,D}$ dependence of I_{on} and V_T computed for the structure in Fig. 3 with $N_{EX} = 4 \times 10^{19}$ and $8 \times 10^{19}\text{cm}^{-3}$, and $X_{J,S} = 3\text{nm}$. The broken lines are for the structure in Fig. 1.

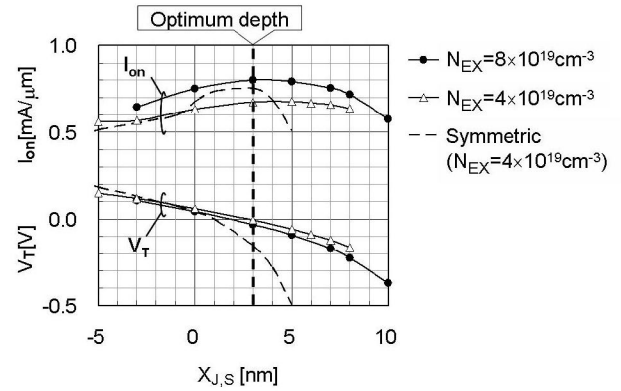

Fig. 7. $X_{J,S}$ dependence of I_{on} and V_T computed for the structure in Fig. 3 with $N_{EX} = 4 \times 10^{19}$ and $8 \times 10^{19}\text{cm}^{-3}$, and $X_{J,D} = -2\text{nm}$. The broken lines are for the structure in Fig. 1.

C. Concept of asymmetric structure

From these observations, the asymmetric structure as shown in Fig. 3 is derived. This structure is topologically similar to V-channel MOSFETs[8] since it has one concave portion in the channel. However, by virtue of the "main" (flat portion) channel being parallel to the surface of the substrate, silicon-on-insulator substrates and various kinds of booster technologies such as hybrid-orientation and embedded source/drain technologies are potentially applicable to this structure.

IV. Discussion

Difficulties in interpreting the simulation results in this work lie in the continuum model of impurity distributions and the carrier transport models used. Regarding the discrete dopant distributions, the optimum junction depth of 2nm derived for the symmetric structure is comparable to the average distance between adjacent impurity ions at the doping concentration of $4 \times 10^{19}\text{cm}^{-3}$. Therefore, the junction depth at the gate corners and thus the corner potential may fluctuate within a gate electrode in the actual devices. Simulation using the DD and the HD models seems to overestimate the diffusion current due to the steep gradient in the carrier concentrations near the source-side corner, as shown in Fig. 5(b). These problems need to be addressed to improve the reliability and accuracy of the estimated device performance.

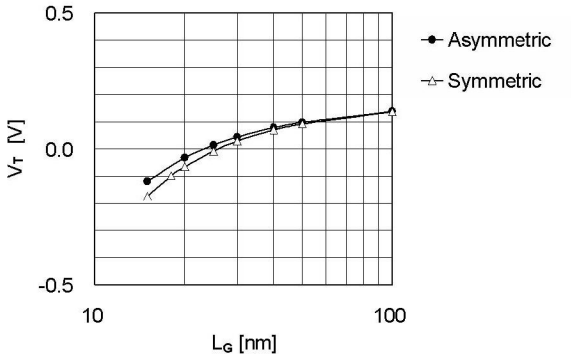

Fig. 8. V_T roll-off curves for the symmetric structure in Fig. 1 and the asymmetric structure in Fig. 3 computed with the design parameters shown in the respective figures.

V. Conclusion

For symmetric planar MOSFETs with extremely shallow junctions, junction depth tolerance must be reduced to about $\pm 1\text{nm}$ in order to control V_T and maintain sufficient current drivability. The proposed asymmetric structure enables use of the potential barrier at the gate corner for SCE suppression without reducing current drivability, and, in addition, increases junction depth tolerance by a factor of three. This structure is therefore a promising candidate for 32nm-node MOSFETs.

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