A Full 3D TCAD Simulation Study of Line-Width Roughness Effects in 65 nm Technology

Luca Sponton*, Lars Bomholt†, Dipankar Pramanik‡, and Wolfgang Fichtner*†
*Integrated Systems Laboratory, ETH, Zurich
†Synopsys Switzerland LLC, Zurich
‡Synopsys, Inc., Mountain View

***Abstract*— For the 65nm technology node and beyond, new manufacturability problems are arising that strongly impact device and circuit behavior. Among these problems, line-edge and line-width roughness (LER and LWR) are of particular interest as dominant issues affecting parametric yield. In this paper, we investigate LWR effects by applying latest generation, full 3D TCAD technology including lithography simulation. In addition, our results answer open questions concerning the applicability of 2D slicing approximations vis a vis a 3D modeling effort. While LWR has been investigated by TCAD before, our methodology includes a full 3D process simulation (including lithography) without simplifications to generate the final transistor structures.**

I. Introduction

Due to the imperfect nature of the lithographic pattern definition and transfer processes, designed mask geometries and final feature shapes on the Si wafer are different and can affect parametric yield [1]. To counteract these unwanted losses in pattern fidelity, OPC (Optical Proximity Correction) and RET (Resolution Enhancement Technology) have become standard CAD technologies. Nevertheless, for sub-100nm technologies, "straight" lines on the mask end up as wobbly features on Si. At the gate level, the imperfect printing process translates into polysilicon features with fluctuating edge shapes and line widths (i.e. LER and LWR).

In this paper a complete simulation flow based on 3D TCAD including lithography is presented (Figure 1). It is used to study quantitatively the impact of LWR on the characteristics of a MOS transistor in the process development phase. The generation of an accurate and robust model based on three-dimensional implantation and diffusion is necessary for small geometry devices, where the process variability meets design variability creating subtle interdependencies.

Moreover, the approach based on simulation allows to decouple the effects of lithography from other phenomena (narrow width effects, stress) which characterize small transistors, while measurements do not offer this possibility. In the second part of the paper the model obtained is therefore used to analyze the validity of the widely accepted slice approximation in a quantitative way, and to explore its unavoidable limits.

II. Three-dimensional device creation

For the creation of the 3D structures, a transistor from an actual 65 nm 4x2 AND gate design was chosen.

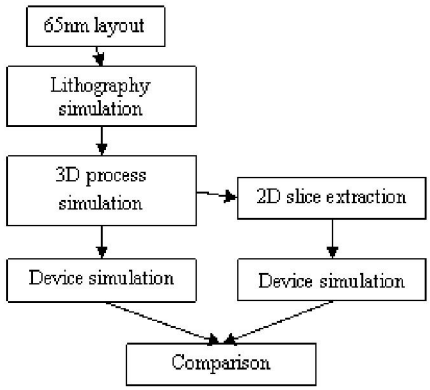

Fig. 1. Simulation flow.

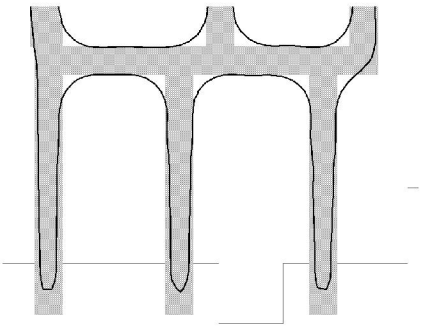

Fig. 2. Particular of simulated contour of the AND gate.

This cell is processed with a lithography emulation tool, which calculates the aerial image: The optical system modeled in this experiment has λ = 193 nm, NA = 0.85 and σ = 0.8, with no defocus. The results of the lithography simulation are shown in Figure 2. The flaring of the transistors coming from the projection of the original layout is problematic, so OPC was applied to the polysilicon mask to improve the printing (Figure 3). Moreover, the effect of defocus on the OPC mask was considered with the simulation of a 150 nm deep defocus. The rightmost NMOS transistor in Figure 3 was chosen for the simulations in the above mentioned situations: projection of the original mask, of the mask corrected by means of OPC and of the corrected mask with a defocus.

Aim of the device creation was to reproduce the influence of

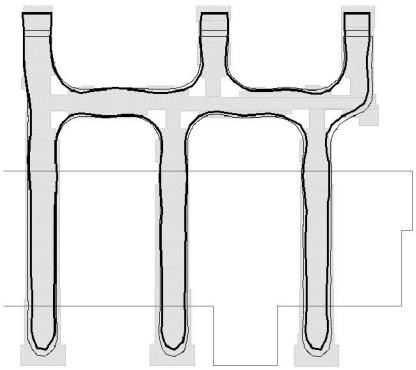

Fig. 3. Same cell magnification processed with OPC. Two contours are visible: the external one is with null defocus and the internal (bold) one is simulated with a defocus of 150 nm.

TABLE I
TRANSISTOR DETAILS

Device	Average L [nm]	σ [nm]	Width [μm]	V_T [V]
Nominal	65	0	0.31	0.392
Flared	48.38	5.73	0.31	0.384
OPC-corrected	65.7	1.8	0.31	0.392
Defocused	52.98	4.33	0.31	0.42

a real 3D mask on the process, mainly in terms of the resulting 3D dopant profiles. The device is set up using the 3D implantation and diffusion facilities given by the process simulator [2]. This approach is definitely more computationally expensive but it takes into account implantation scattering and state-of-the-art point-defect diffusion models. We did not include shallow trench isolation in the simulation domain in order to separate the effects of lithography from other 3D effects. A sidewall oxide of 7 nm thickness and conformal nitride spacers of 70 nm thickness have been used. Dimensions of these features have been previously obtained with 2D process simulations. The process flow used to simulate the device is a generic 65 nm one, which is calibrated on literature and measurements data.

Figure 4 shows the results of the process simulation in the case of the flared transistor (contour from the original cell). It can be seen that the doping profile on the channel surface follows the gate shape. Implantation scattering and thermal diffusion act as a low pass filter only on very rough gate edges [3], while in the case of optical-generated roughness, the variation is smooth along the width of the transistor. The OPC mask generates an almost straight gate, as it is possible to see from Table I, while the defocused structure has an average gate length 20% smaller compared to the straight gate.

In Figure 5, it is possible to see the boron concentration immediately under the gate oxide (0.1 nm) in the flared transistor: The short channel boron pileup effect is visible in the narrower part of the transistor. The boron concentration under the oxide/silicon interface is of the order of 3-4e18 cm^{-3}

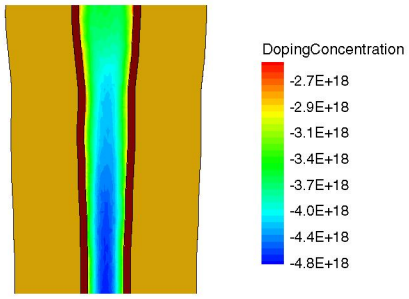

Fig. 5. Flared transistor channel doping concentration (cut taken 1 Å under oxide/silicon interface).

which gives a threshold voltage in the order of 0.4 V for the various transistors simulated here (Table I).

III. ELECTRICAL SIMULATION

To achieve accurate results in the electrical simulation the channel volume of the devices has been extremely refined with a 0.1 nm vertically spaced mesh. As far as the physical models are concerned, only the Poisson, electron, and hole equations have been solved. Typical physical effects (degradation of mobility due to normal fields and high-field velocity saturation) have been included in the simulation. Figure 6 shows the threshold characteristics in four different cases. The case in which no lithography simulation is applied (straight gate) is consistent with a 2D simulation, where the width is considered a scaling factor[1].

As it is clear from the different simulations, lithography effects play an important role in the final device characteristics. They impact the threshold voltage of the various transistors, as shown in Figure 6. The threshold voltage of the defocused device is higher than the OPC-corrected device. This is due to the higher concentration of boron in the channel for that particular transistor. A comparison of the saturation currents of the various transistors shows a behavior similar to the one seen for low drain voltage, the flared transistor carrying 15% more current than the OPC-corrected one (Figure 7). For high drain bias the OPC-corrected transistor behaves closely to the ideal one: The high longitudinal fields compensate for the slight differences in the gate length.

The subthreshold current for the four different transistors is shown in Figure 8. The flared gate transistor is again driving almost one order of magnitude more current with respect to the ideal or the OPC-corrected one. From electrical simulations, it is clear that OPC is mandatory in order to obtain a device whose characteristics are close to the ideal straight-gate case: on the other hand, a defocus in the projection can also alter the performance of an OPC corrected cell significantly.

[1]For consistency, also for this device, a full 3D simulation was performed.

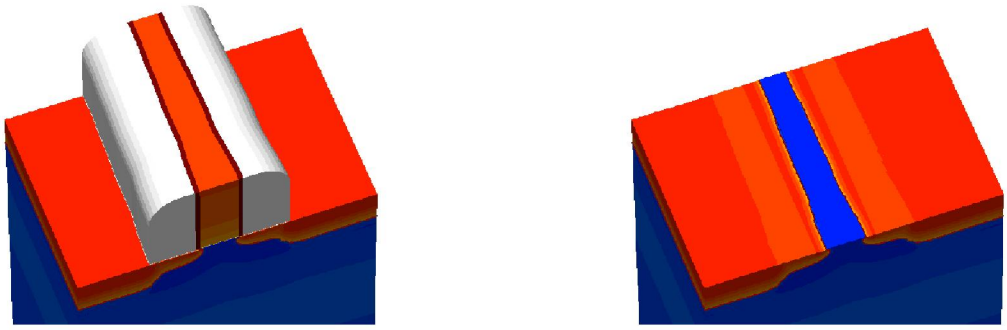

Fig. 4. Three-dimensional process simulation results: (left) with gate stack and (right) silicon only.

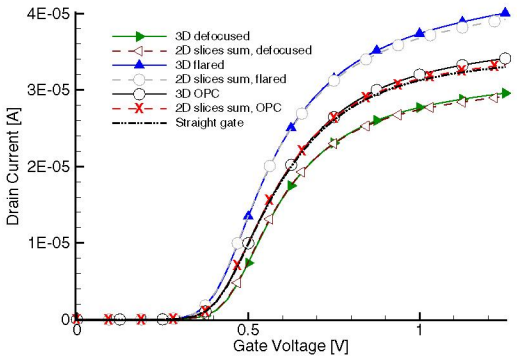

Fig. 6. Comparison of $I_d - V_g$ curves for the simulated 3D transistors, drain bias is 50 mV. Dashed lines represent the slice approximation.

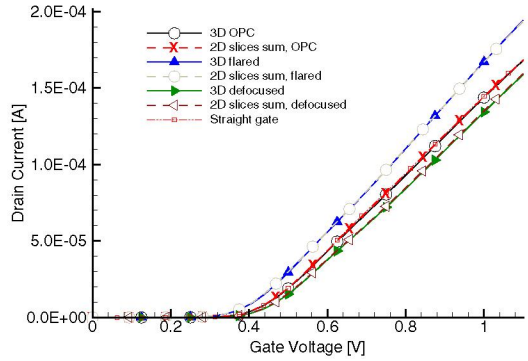

Fig. 7. Comparison of $I_d - V_g$ curves at high drain bias (1.25V). Dashed lines represent the slice approximation.

IV. The slice approximation of a transistor

The three-dimensional simulation of a transistor is a demanding task, and it cannot be used to simulate even small circuits because of the computational time requirements. There is, therefore, the necessity of using a more affordable simulation technique to take into account the effects of lithography on the behavior of the transistor in the case of more than one isolated device. Approximating a transistor whose gate length is not constant using a parallel of transistors of different lengths is a commonly used procedure [4], [5]. It consists of considering a certain number of slices of the original devices in such a way that the final device characteristics are given by the sum of the individual slice characteristics. The gate length is clearly approximated as constant for each slice, so we can write:

$$I_{on} = \sum_i I_{on,i} \Delta W_i$$

and so on, where the i^{th} 2D simulated slice is normalized to 1 μm and ΔW_i is its actual width.

This approximation is applicable only if the current flow is linear, which means there should not be relevant current components in the third dimension due to the gate shape. This assumption is checked directly from the 3D simulations and in Figure 9 the current flow has been highlighted by stream-traces in the channel. Two-dimensional slices are not simulated from scratch, but they are taken from the 3D structure so that there is no profile difference due to different grid adaptations in 2D or 3D. Again, to avoid reinterpolation of the doping levels, we cut the 3D structure on grid planes. In this way the node values are exactly the same in the cutting plane of the original structure and in the 2D slice. After that, the slices are remeshed using the same grid refinements as in 3D not to introduce any difference for the electrical simulation.

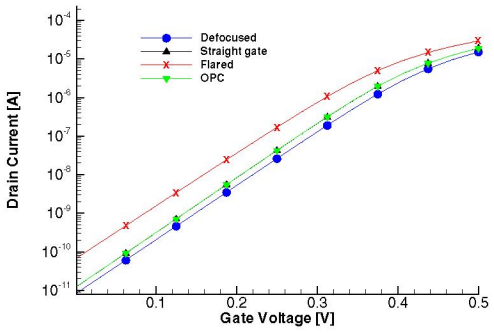

Fig. 8. Subthreshold currents.

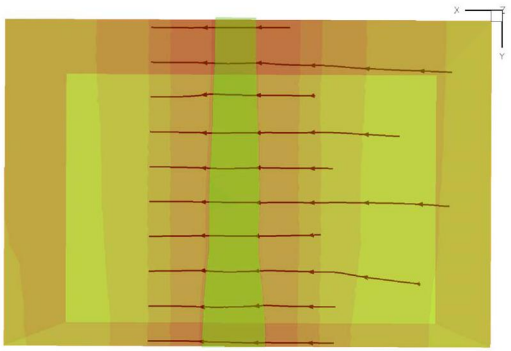

Fig. 9. Current stream traces in the flared 3D structure, view from the top.

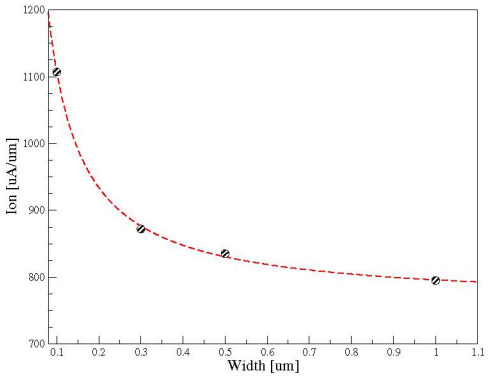

Fig. 10. Saturation current density variation vs width of the device. The dashed line is a fitting of the 3D simulation points.

The mesh refinement level (number of points) to use in these simulations is an important issue. Too coarse a 3D mesh leads to an overestimation of the current compared with 2D simulated slices. A very fine mesh is necessary in the regions that are physically relevant for the simulation (channel and extensions up to the contacts) in order to obtain stable results.

The electrical device simulations of the slices cut from the 3D transistors have been made under the same conditions described for the full structure. Current values were then normalized and summed to obtain the total current that has to be compared with the 3D simulation. In Figure 6 and Figure 7 the results are reported. There is good agreement between 3D simulations and their slice approximation counterparts, with a slight maximum error of $\sim$2% only at low drain bias (linear region).

V. Limits of the slice approximation approach

The slice approximation described above is not valid in all situations. In the case of a narrow-width transistor, the interaction of the sides and shallow trench isolation both from a process and an electrical point of view are 3D effects that cannot be modeled by simple 2D slices. It is not trivial to identify the point at which the slice approximation fails, as the onset of the inverse narrow width effect (INWE) [6] is strongly dependent on the process conditions and the geometry of the device, and it is also modulated by the channel length [7]. In Figure 10, a 3D simulation study of the INWE on the saturation current for the 65 nm technology used in this paper is reported. Details of this study are outside the scope of this paper; however, it is evident that the width of the transistor has a major influence on the characteristics when going under 0.3 μm (difference $> 10\%$). In the case of a very narrow transistor, nothing but the full three-dimensional approach can give an accurate insight into the device physics.

Another issue not accountable with the 2D slice approximation is the stress coming from the third dimension, which can drastically change the transistor characteristics again, in particular, for narrow transistors. Nevertheless, as the stress affects essentially the carrier mobility in the channel, its effect can be accounted for by modifying the mobility parameters of the various slices according to a stress simulation.

VI. Conclusions

In this work we detailed a comprehensive 3D simulation flow to study the impact of line width roughness on a modern transistor. The approach used here is anyway general, because whenever there is the need of addressing small geometries effects, only 3D TCAD simulations allow to have the necessary physical insight on intertwined phenomena and to separate them. The quantitative results obtained in this way allow to substantiate the accuracy of approximations, like the widely used slicing approach, and to explore their limits that are usually dependent on the particular technology investigated. Our study shows that while being a cheap and accurate alternative to 3D simulation for wide transistor, the slice approximation fails to give predictive results for narrow transistors that are commonly used in recent designs and has therefore to be applied carefully.

Acknowledgments

The authors would like to thank Arsen Terterian, Yves Saad, Alessandro Nannipieri, and Gyorgy Kiralyfalvi from Synopsys Switzerland LLC for their support and useful discussions during the development of this work.

References

[1] J.-Y. Lee, J. Shin, H.-W. Kim, S.-G. Woo, H.-K. Cho, W.-S. Han, and J.-T. Moon, "Effect of line edge roughness (ler) and line width roughness (lwr) on sub-100 nm device performance," in *Proceedings of SPIE*, vol. 5376, 2004, pp. 426–433.

[2] *Synopsys Sentaurus TCAD Manuals*, Synopsys Switzerland LLC, Oct 2004.

[3] S. Xiong and J. Bokor, "A simulation study of gate line edge roughness effects on doping profiles of short-channel mosfet devices," *IEEE Transactions on Electron Devices*, vol. 51, no. 2, pp. 228–232, Feb. 2004.

[4] P. Oldiges, Q. Lin, K. Petrillo, M. Sanchez, M. Ieong, and M. Hargrove, "Modeling line edge roughness effects in sub 100 nanometer gate length devices," in *Proceedings of SISPAD*, Sep 2000, pp. 131–134.

[5] A. Shibkov and V. Axelrad, "Integrated simulation flow for self-consistent manufacturability and circuit performance evaluation," in *Proceedings of SISPAD*, Sep 2005, pp. 127–130.

[6] L. A. Akers, "The inverse-narrow-width effect," *IEEE Electron Device Letters*, vol. EDL-7, no. 7, pp. 419–421, July 1986.

[7] T. Oishi, K. Shiozawa, A. Furukawa, Y. Abe, and Y. Tokuda, "Isolation edge effect depending on gate length of mosfets with various isolation structures," *IEEE Transactions on Electron Devices*, vol. 47, no. 4, pp. 822–827, Apr. 2000.

