3-D Process Simulation of CMOS Inverter Based on Selete 65nm Full Process

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***Abstract*—We have succeeded in 3-D process simulation of a CMOS inverter based on the Selete 65nm full process. In particular, we have focused on the robustness and the availability of the process simulator HySyProS (Hyper Sythesized Process Simulator).**

Key words: 3-D process simulation, CMOS-inverter, CMOS full process

I. INTRODUCTION

In ULSI logic devices, the characteristics of CMOS inverter is one of the important indices. As ULSI devices have been becoming finer, the delay time (tpd) of CMOS inverters and its variation have strongly affected circuit designs and defect rates of ULSI. Process simulators are very useful to analyze directly its process variation and the relation between the characteristics of inverter and process conditions.

Until now, CMOS inverters have been analyzed with circuit simulators [2], 2-D process/device simulators [3],[4], [5] or only 3-D device simulators[6], however, 3-D process simulation of the CMOS full process has not been realized. One of the problems is the robustness of the 3-D process simulator, in particular 3-D mesh and 3-D topography. Another problem is the need for an enormous amount of memory and calculation time. We have developed a 3-D process simulator, HySyProS, which has robust topography calculation and meshing, and includes functions to reduce memory needs and calculation time.

In reality, HySyProS is a 3-D impurity simulator which includes implantation (analytical/Monte-Carlo) models, diffusion (Fair, Mulvaney, Dunham's 3/5-stream) models, an oxidation (visco elastic) model and stress analysis model.

In this paper, we present 3-D process simulation results of a CMOS inverter structure and demonstrate its robustness and availability.

II. MESHING AND TOPOGRAPHY MODELS

A. Mesh Classes

HySyProS has two mesh classes, one of which is based on the orthogonal mesh, and includes the irregular (oblique) cuts of the rectangular boxes near the interfaces and the mask boundary. The other mesh class is based on Delanay elements, and is used for implantation, diffusion, oxidation, and stress analysis.

B. Topography Calculation Method

We adopt a very robust and fast method that surface topography is represented as contour surface in a distance function [7], which is different from Sethian's Level set method that solves Hamilton Jacobi's equation [8]. Our method makes it possible to realize the practical topography calculation, which has isotropic/planar/selective depositions, and isotropic/anisotropic/planar /oblique/arbitrary-shape etching.

III. SIMULATION OF A CMOS INVERTER

We use the Selete 65nm full process as process flow, which includes trench isolation, N-well/P-well implantation, channel annealing, gate oxidation, poly-silicon gate patterning, Halo/extension implantation, gate side wall step, source/drain implantation, and source/drain annealing, and final forming contact/Metal(Vdd, Vss, input, and output)/interlayer. The transistor gate length is 50nm and gate widths of nMOS/pMOS are 100nm/200nm. The total number of simulation process steps is 86 (deposition steps:20, etching steps:41, implantation, steps:20, diffuse/oxidation steps:6). The size of the calculation region is 0.41μm × 1.16μm × 2.1μm.

A. Calculation Procedure of the CMOS inverter

In order to reduce the memory and calculation time, half of the region was computed until the source/drain annealing step. Then particularly diffusion steps were simulated for each of the nMOS and pMOS regions. This procedure corresponds not only to the reduction of calculation time but also to that generally calibration parameters are set on each of the nMOS and pMOS regions. The procedure is not related to the characteristics of the inverter, because the boundary of nMOS/pMOS is far from gates and source/drain regions.

B. Results

The simulation results of the basic process steps are shown as 3-D topography in Figs. 1(a), (b), (c), (d), (e) and (f), which correspond to trench isolation, filling trench with oxide film(ASSG), gate oxidation, patterning poly-Silicon gate,

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forming gate side-wall, and contact/Metal(Vdd, Vss, input, and output)/interlayer, respectively. Fig.1 (a) shows 3-D shape after the wall oxidation of the trench, and the zoomed shape of the active silicon area is shown in Fig 2. It can be seen that the oxide near the edge of the active area is a little thicker than the center due to the oxidation. And then, Figs.3(a) and (b) show the average stress on the surfaces of Si and SiO2, respectively. We can see that the oxidation induces tension in Si, and compression in SiO2 at the top corner of trench. On the other hand, compression in Si and tension in SiO2 are induced at the bottom corner of trench. The gate oxide shape of the nMOS is zoomed up in Fig. 4, in which we can find the a little thinning of the gate oxide near the corner of the active area. Even if the calculation region is wide, ultra-thin films less than 2nm can be represented in 3-dimensions. And then, the poly-silicon gate and gate side wall are formed by deposition and etching steps, as shown in Figs.1(d) and (e), respectively. A well-known and difficult problem is to clean up residuals after etching on the fine concave and convex surfaces which is formed by oxidations. We can see that there is no residual of poly-silicon(gate) or Si3N4(side-wall) in Figs. 1 (d) and (e). The impurity distributions after channel annealing step and S/D annealing step are shown in Figs. 5 and 6, respectively. For all the diffusion steps, Muvaney model was used . After the S/D annealing, a reflected structure is added, and then contact/metal/interlayer are formed. The final 3-D topography, 3-D net impurity concentration, 2-D cross sections of the nMOS and pMOS are shown in Fig. 1 (f), Figs. 7(a), (b) and (c), respectively.

The maximum memory is about 10GB at final meshing. The CPU calculation time is about 65,000 sec with AMD opteron2.59GHz . The total number of nodes is 931,153 and the total number of elements is 2,205,249. These results demonstrate that HySyProS can simulate the Selete 65nm full CMOS process in three-dimensional models .

IV. Conclusion

We have realized the 3-D process simulation of the CMOS inverter. The process is based on the 65nm full process of Selete. This demonstrates that HySyProS is very robust and has high availability.

References

[1] T. Wada and N. Kotani, IEICE Trans. Electron., E82-C, pp. 839–847, 1999

[2] Peter M. Lee, proceeding of VPAD, pp.154-155, 1993.

[3] R.E.Bank et al., IEEE Transaction on Electron Devices, vol.ED-32, pp.1992-2007, 1985.

[4] N. Shigyo et al., Technical Report of IEICE, VLD97-53, pp.63-70, 1997, in Japanese.

[5] T.Fukuda et al., JSAP Catalog Number, AP002235, pp.71-76, 2000, in Japanese.

[6] Y. Moreau et al., IEEE Transactions on Nuclear Science, vol.42, pp.1789-1796, 1988.

[7] T. Uchida et al., Technical Report of IEICE, VLD2001-76, pp.19-24, 2001, in Japanese.

[8] J.A. Sethian and D. Adalsteinsson, IEEE Trans. On Semiconductor Manufacturing, Vol.10, No.1, pp.167-184, 1997.

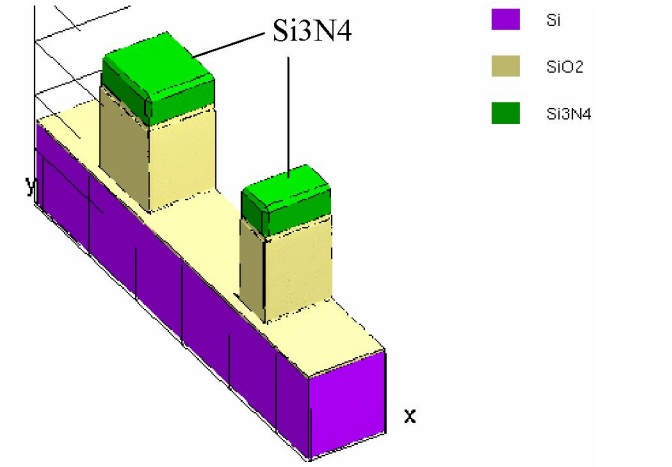


Fig. 1 (a) 3-D view of the trench oxidation

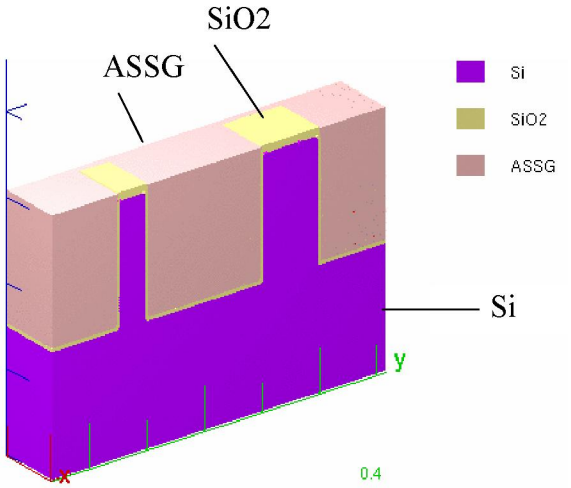


Fig1 (b) 3-D view of the filled trench with ASSG

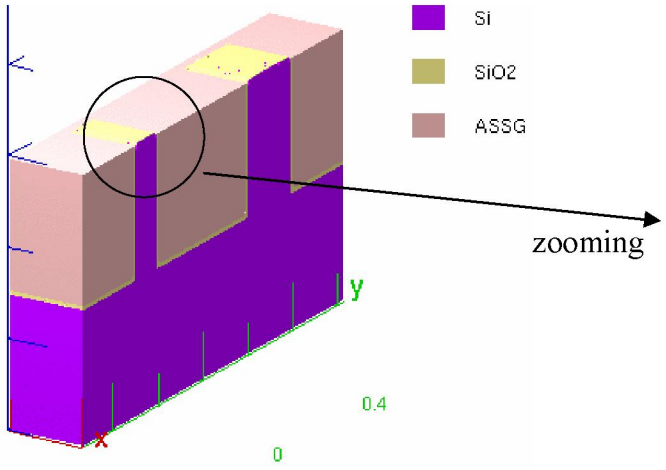


Fig. 1(c) gate oxidation step (3-D view)

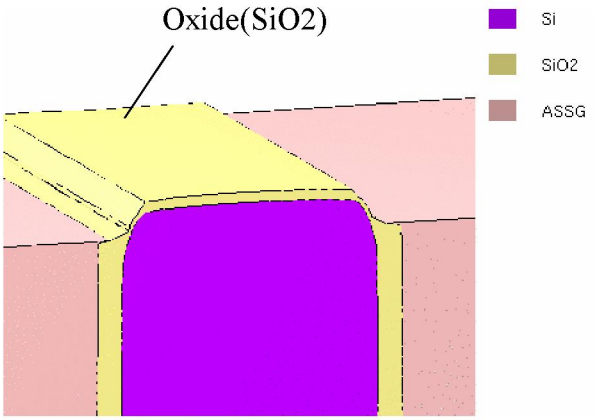


Fig.4 zoomed gate-oxide film of nMOS

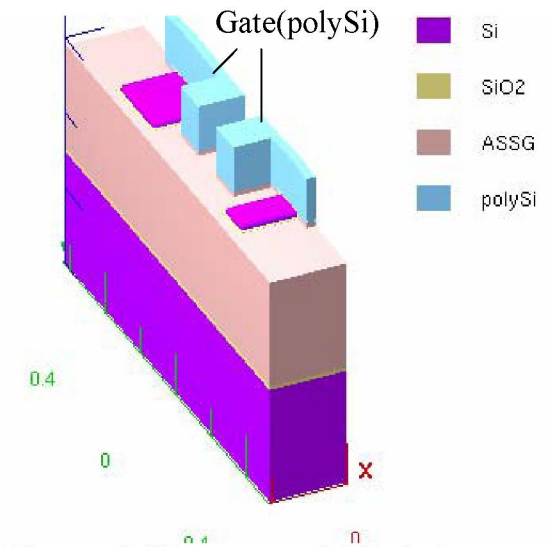


Fig. 1(d) gate polySilicon patterned (3-D view)

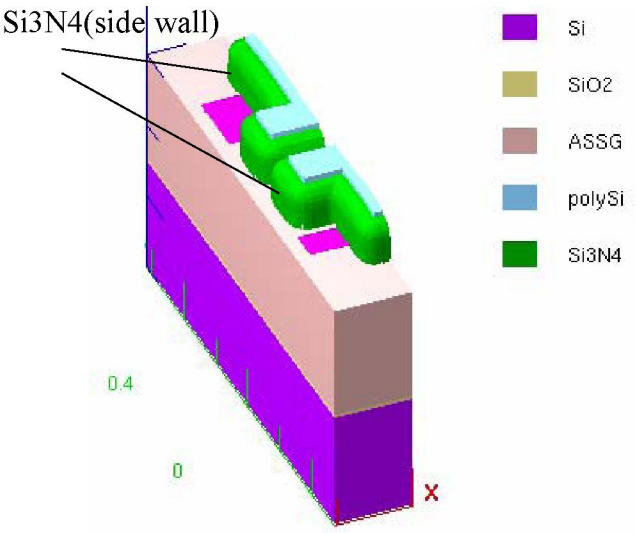


Fig. 1(e) forming gate side wall (3-D view)

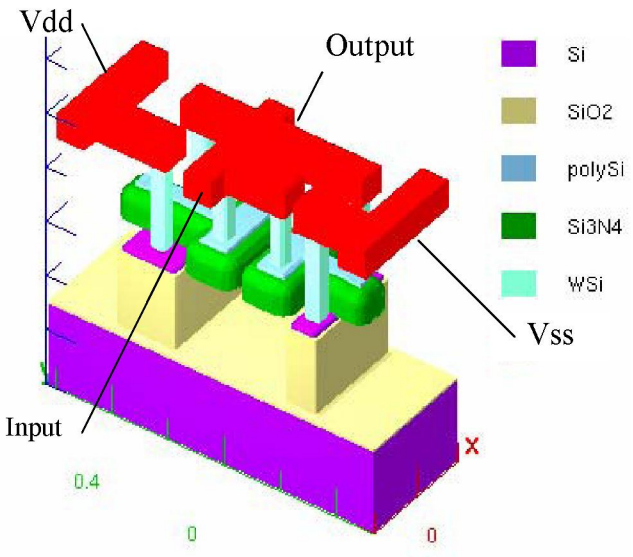


Fig.1(f) forming contact/Metal/interlayer

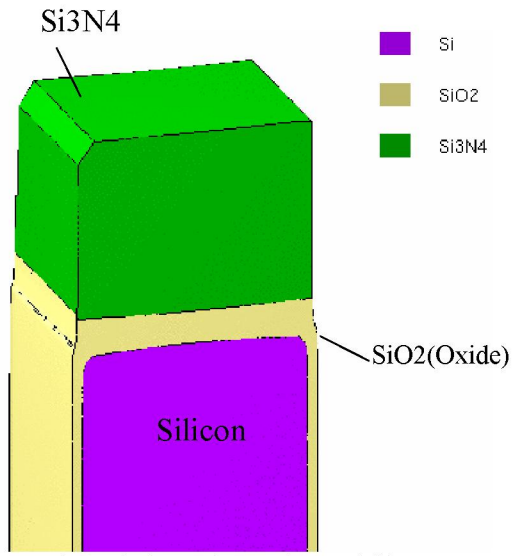


Fig. 2 3-D view of the active region and Si3N4

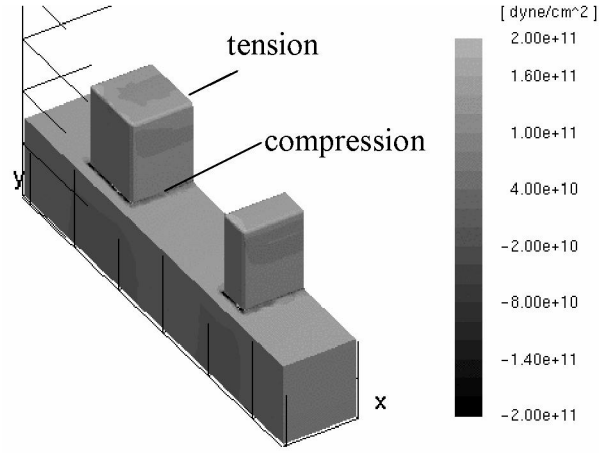


Fig. 3 (a) Average stress on Si

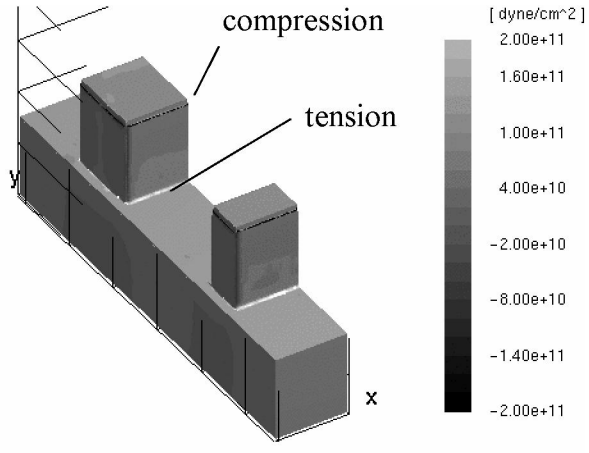


Fig. 3 (b) Average stress on SiO2

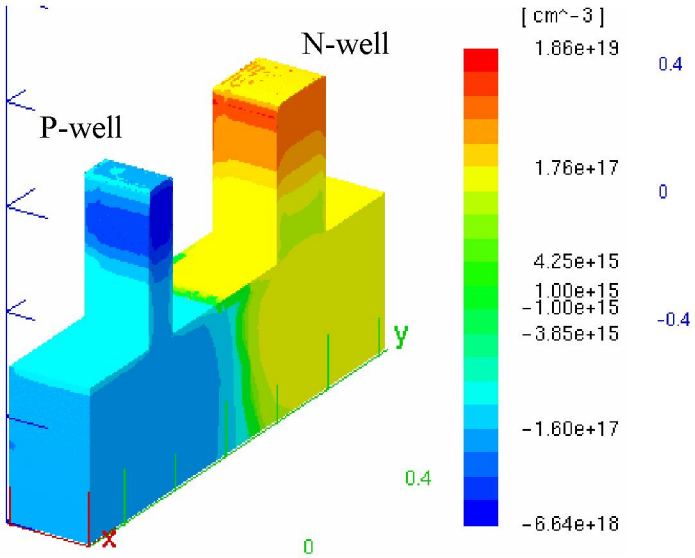


Fig. 5 Net impurity distribution at the channel annealing step

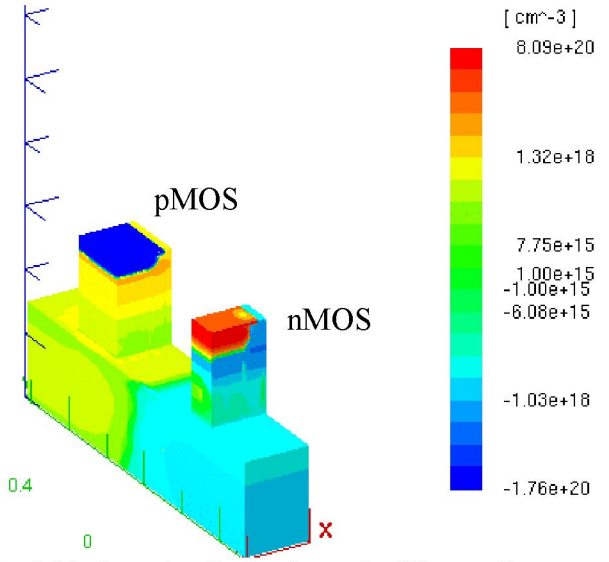
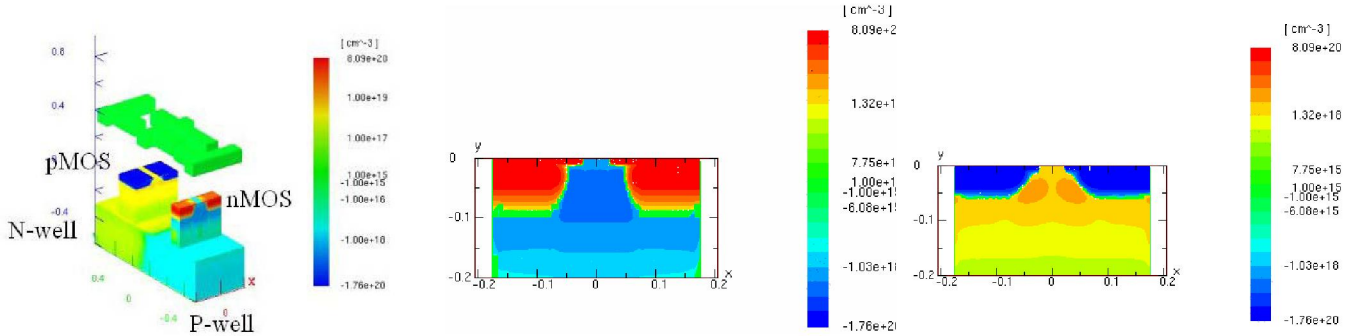


Fig. 6 Net impurity distribution at the SD annealing step



(a) 3-D impurity concentration (b) 2-D cross section of nMOS (c) 2-D cross section of pMOS

Fig. 7 Final net impurity concentration